

# LCFC Confidential

## YOGA3-BDW M/B Schematics Document

INTEL Broadwell Mobile ULT Platform

INTEL BDW U-series CPU + DDR3L DIMM+ NV N16S-GT

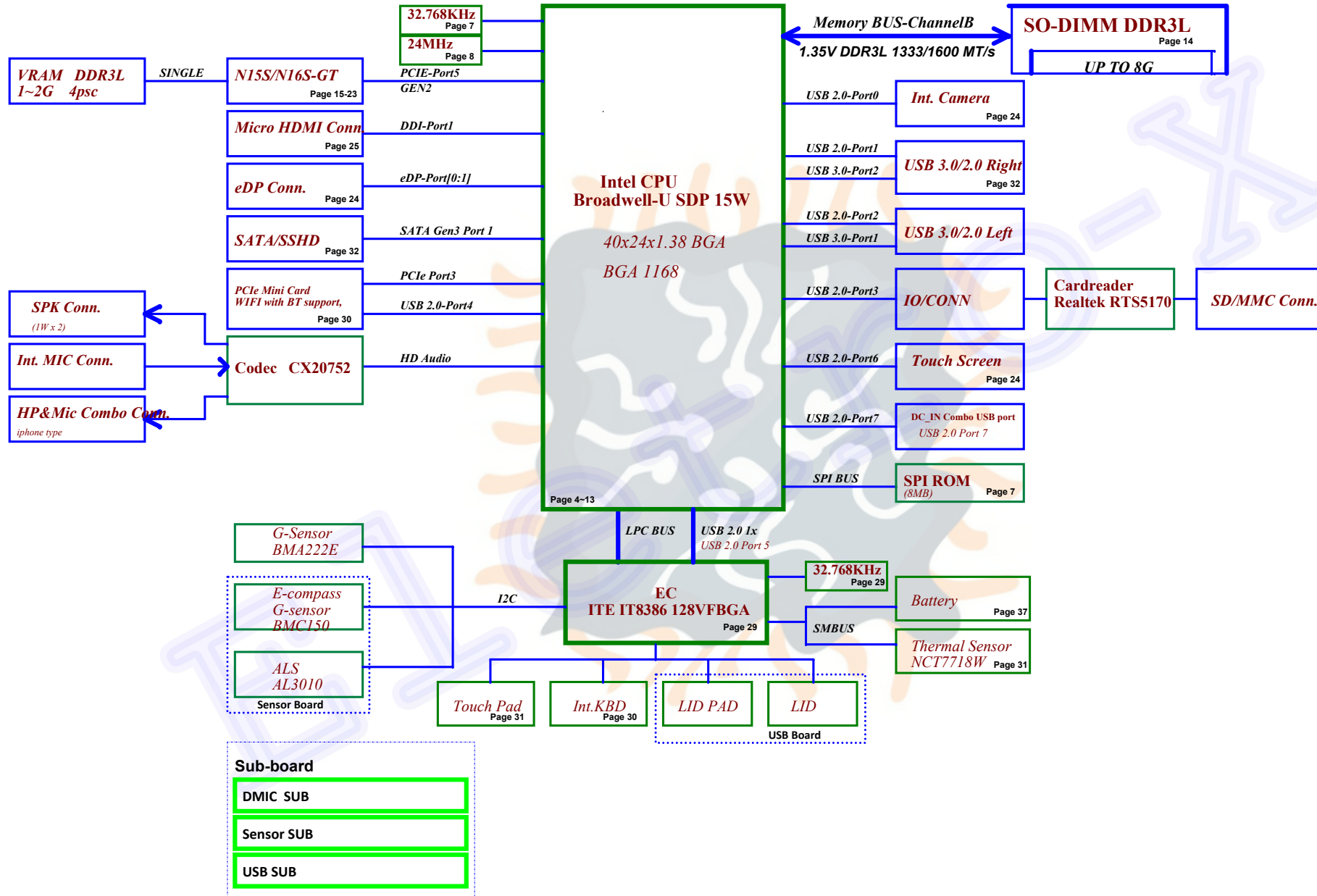
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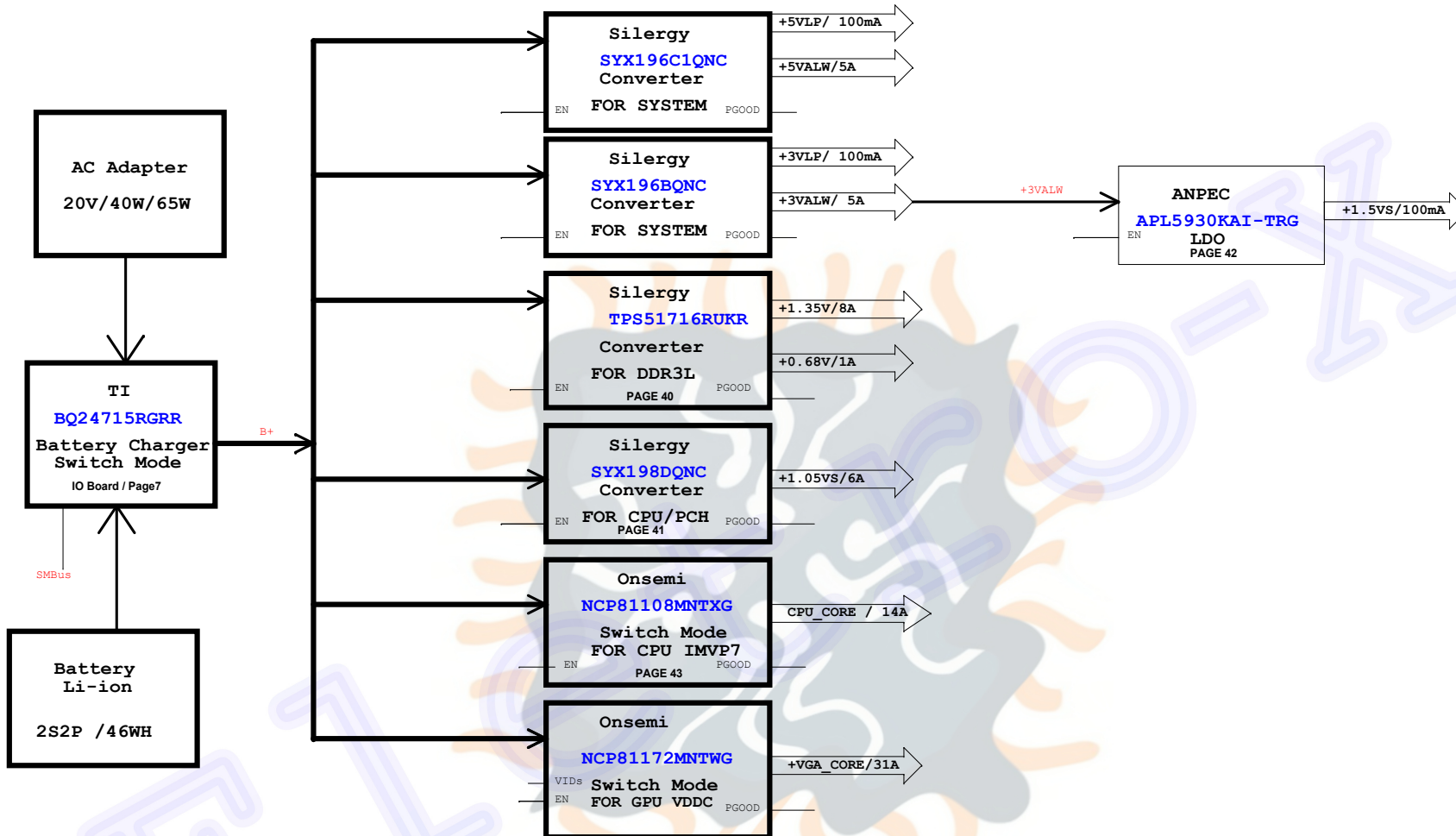
REV:1.0

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# Yoga3 BDW Refresh Block diagram





Power Plane State	B+ +3VL +5VLP	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS +CPU_CORE	+1.35V_CPU
S0	O	O	O	O	O	O
S3	O	O	O	O	X	O
DS3	O	O	X	O	X	X
S5 S4/AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
DS3 (Suspend to RAM)	LOW	LOW	HIGH	ON	LOW	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

### ***SMBUS Control Table***

	SOURCE	Sensor	ALS	BATT	touch sensor	SODIMM	GPU	Thermal Sensor	PCH	charger
EC_SMB_CLK1 EC_SMB_DAT1	IT8386 +3VALW_EC	X	X	V +3VLP	X	X	X	X	X	V
EC_SMB_CLK3 EC_SMB_DAT3	IT8386 +3VS	V +3VS	V +3VS	X	X	X	X	X	X	X
EC_SMB_CLK0 EC_SMB_DAT0	IT8386 +3VS	X	X	X	X	X	V	V +3VS	V +3VALW_PCH	X
SMB_CLK SMB_DATA	PCH +3VALW_PCH	X	X	X	X	V +3VS	X	X	X	X

### SM Bus address

	Device	address
EC1	Battery	0001_011X b
	Charger	
EC3	Sensor	
	ALS	
EC0	Thermal Sensor	1001_100xb
	PCH THM	
PCH	TP	

## PCIE PORT LIST

Port	Device
1	<i>X</i>
2	<i>X</i>
3	<i>WLAN</i>
4	<i>X</i>
5	<i>GPU</i>

### USB Port Table

USB20		USB30	
0	CAMERA	1	Left USB
1	Right USB	2	Right USB
2	Left USB	3	x
3	CARD READER	4	x
4	BT		
5	Sensor		
6	TOUCH PANEL		
7	DC_IN combo USB2.0		

### BOM Structure Table

BOM Structure		BOM Structure	
DA8@	PCB	MIRROR@	EC Mirror-code enable
UMA@	UMA SKU part	UNMIRROR@	EC Mirror-code disable
DEBUG@	DEBUG CARD Part	OPT@	Discrete GPU SKU part
ME@	ME part(connector, hole)	N15SGT@	For N15S-GT GPU part
RF@	RF request	GC6@	GC62.0 support part
EMC@	EMC request	RANKA@	For VRAM RankA part
CD@	COST DOWN Part		
REV@	RESERVER Part		










### BOM Configuration Table


[illegible]

### X76&VGA Configuration Table

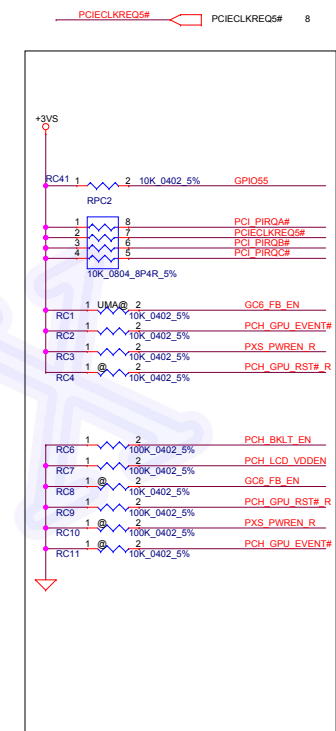
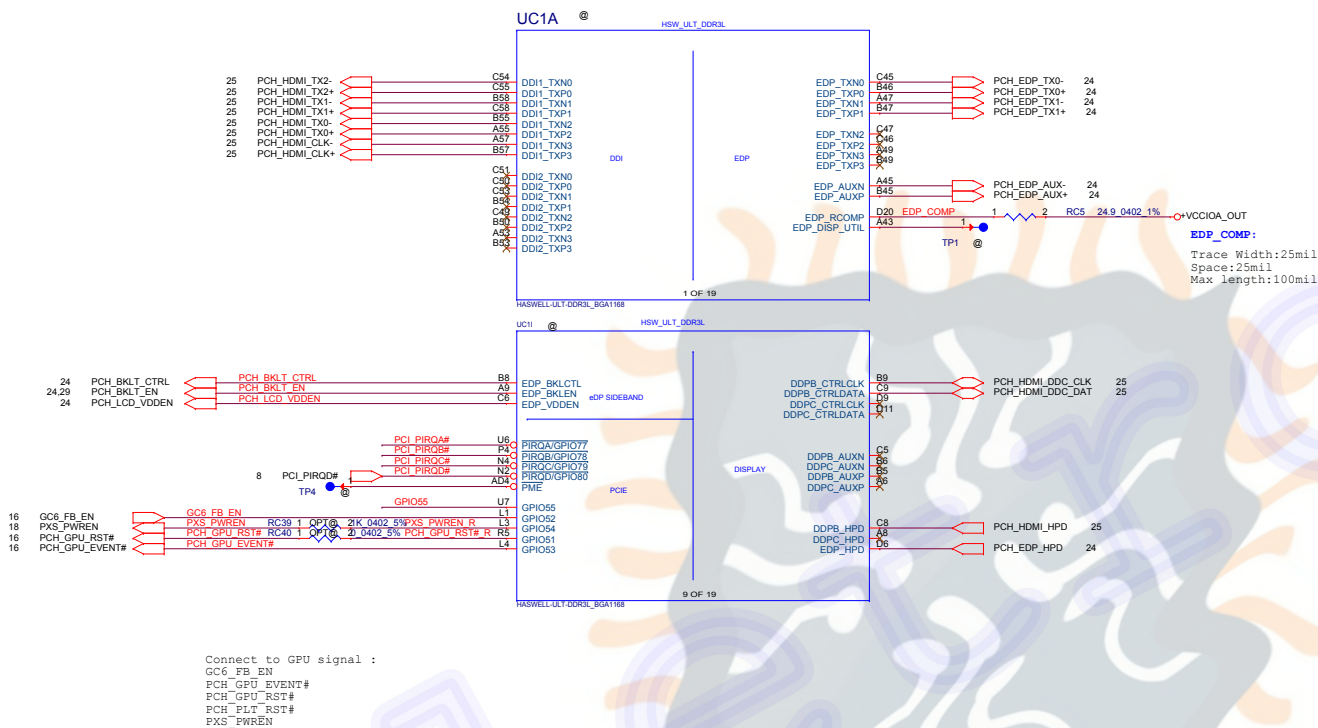
[illegible]

## PCB And LOGO Config

<b>PCB</b>	 <p>PCB 0YC NM-A381 REV0 M/B</p>	<div>   </div>
<b>CPU</b>	<div>    </div> <p>BDW U2+2 Ci7      BDW U2+2 Ci5      BDW 2+2U 1.6G 1333 ES2</p>	
<b>VRAM</b>	<div>    </div> <p>HYNIX 2G      MICRON 2G      SAMSUNG 2G</p>	

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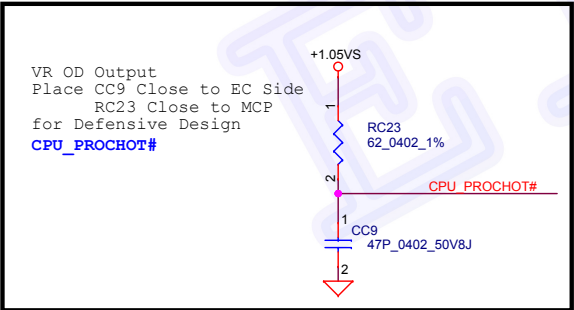
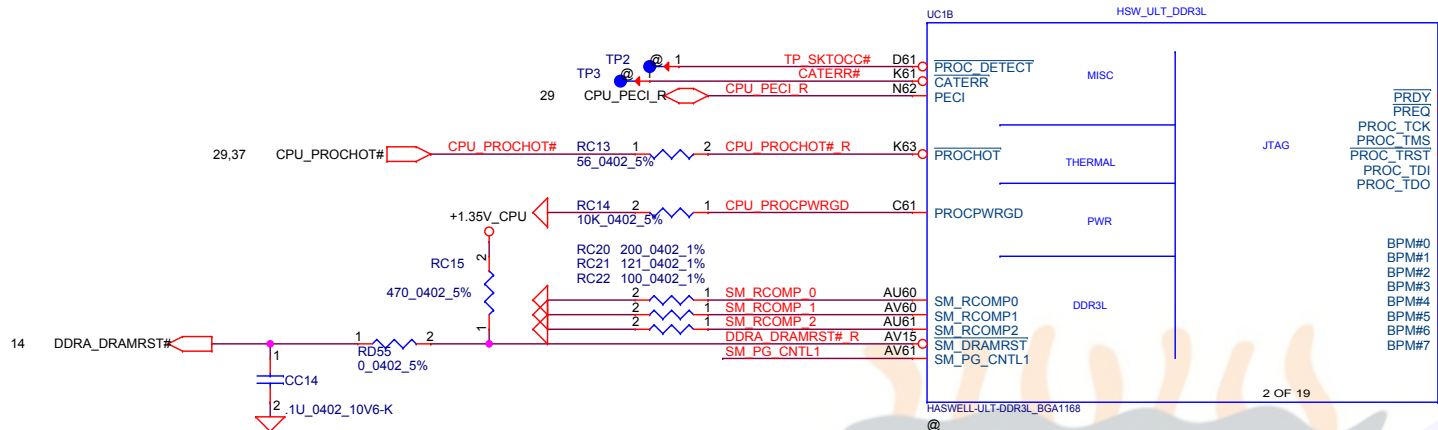





Port	DDI PROCESSOR Pin Names	HDMI* Mapping
Port 1	DDI1_TXN[0]	HDMIx_C_TX2_DN
	DDI1_TXP[0]	HDMIx_C_TX2_DP
	DDI1_TXN[1]	HDMIx_C_TX1_DN
	DDI1_TXP[1]	HDMIx_C_TX1_DP
	DDI1_TXN[2]	HDMIx_C_TX0_DN
	DDI1_TXP[2]	HDMIx_C_TX0_DP
	DDI1_TXN[3]	HDMIx_C_CLK_DN
	DDI1_TXP[3]	HDMIx_C_CLK_DP
	DDPB_HPD	DDI1_HPD_0
	DDPB_CTRLCLK	DDI1_CTRL_CK
	DDPB_CTRLDATA	DDI1_CTRL_DATA

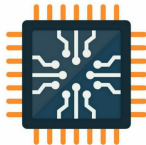
Fin Name	Recommendation
DDPC_AUXP	No Connect
DDPC_AUXN	No Connect
DDPC_HPD	No Connect
DDI2_TXP[3:0]	No Connect
DDI2_TXN[3:0]	No Connect
DDPC_CTRLCLK	No Connect
DDPC_CTRLDATA	No Connect



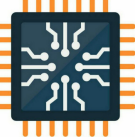


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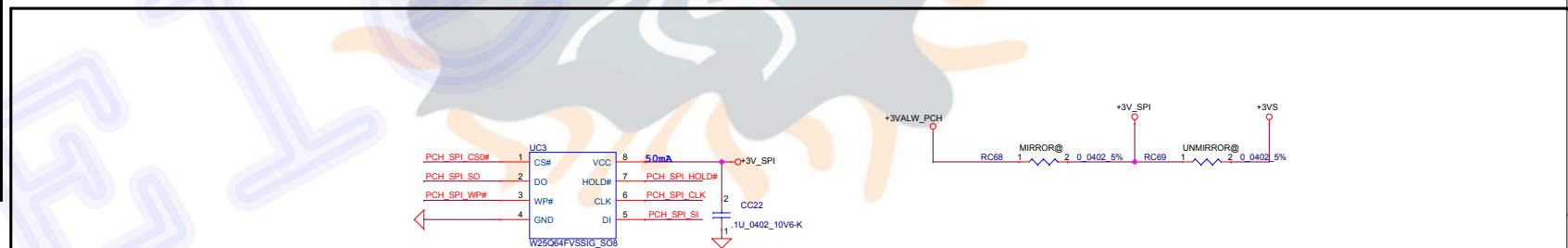
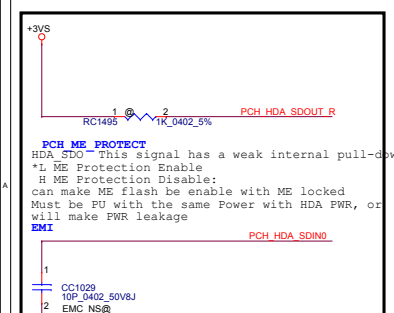
Title		
MCP (MISC,THERMAL,JATG) <b>LCFC</b>		
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
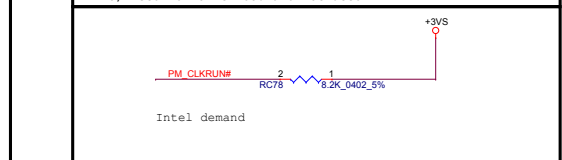


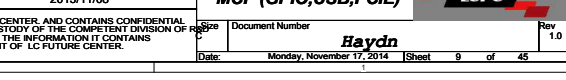
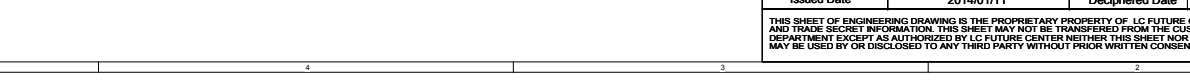
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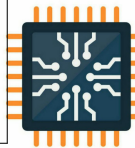
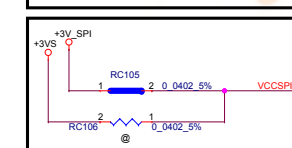
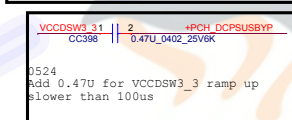
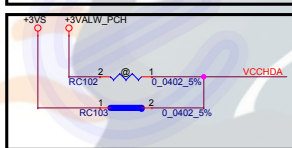
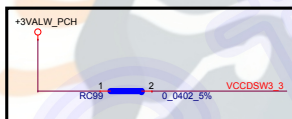
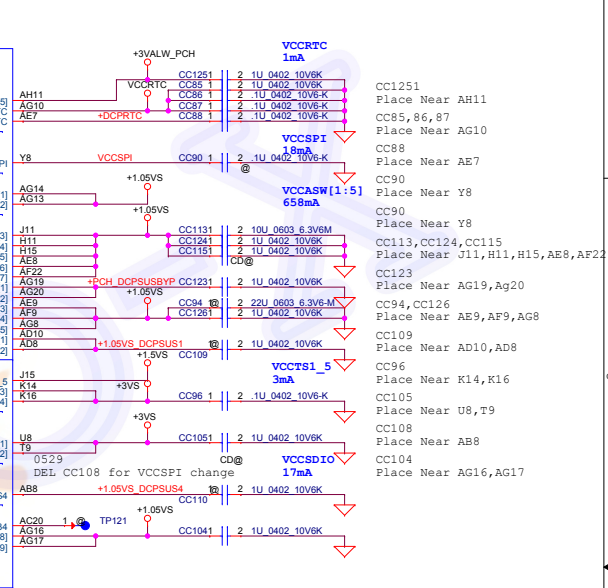
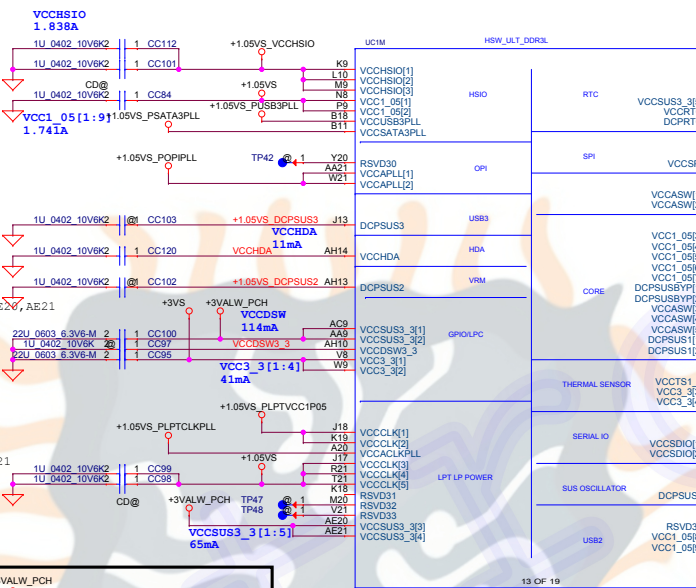
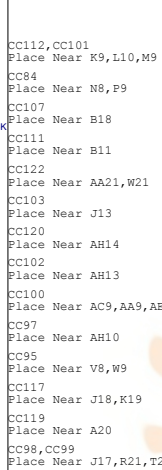
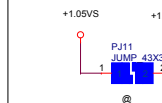
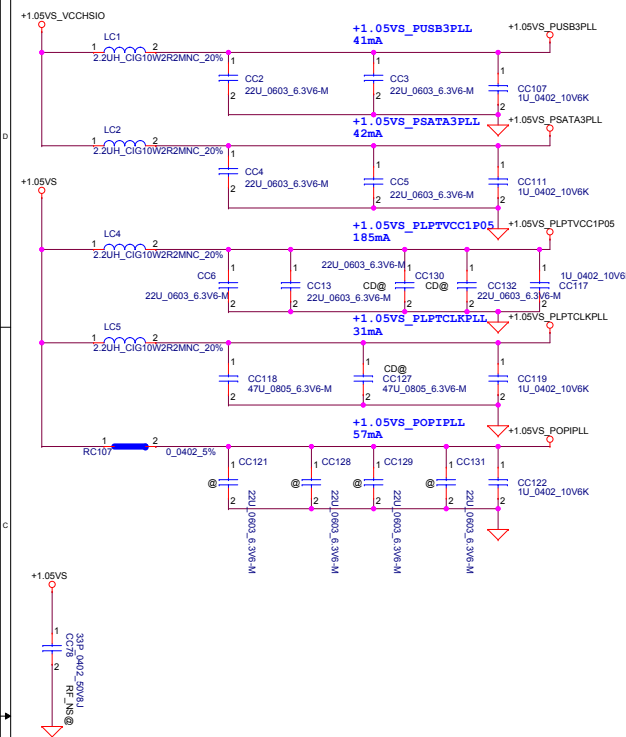


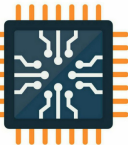
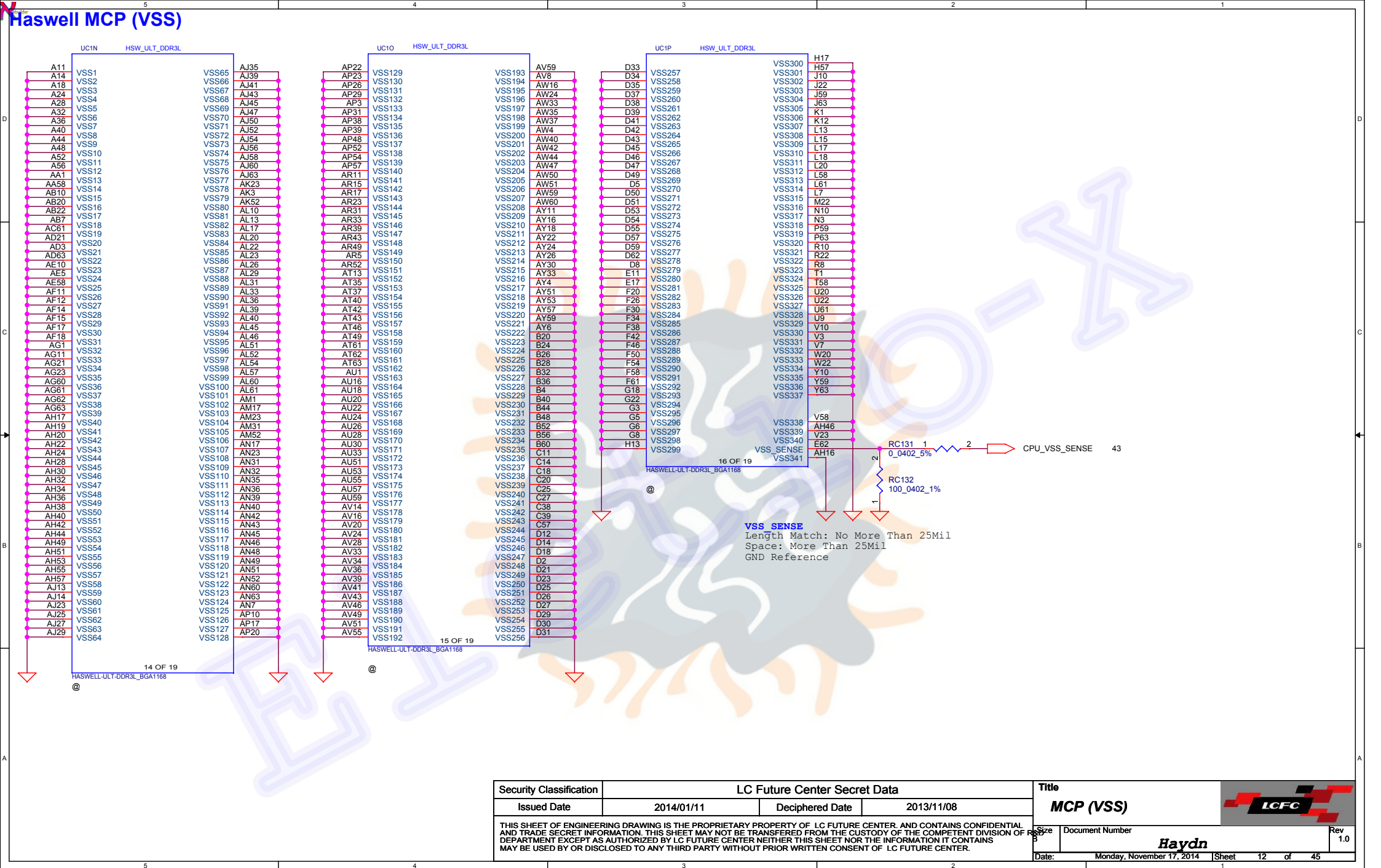




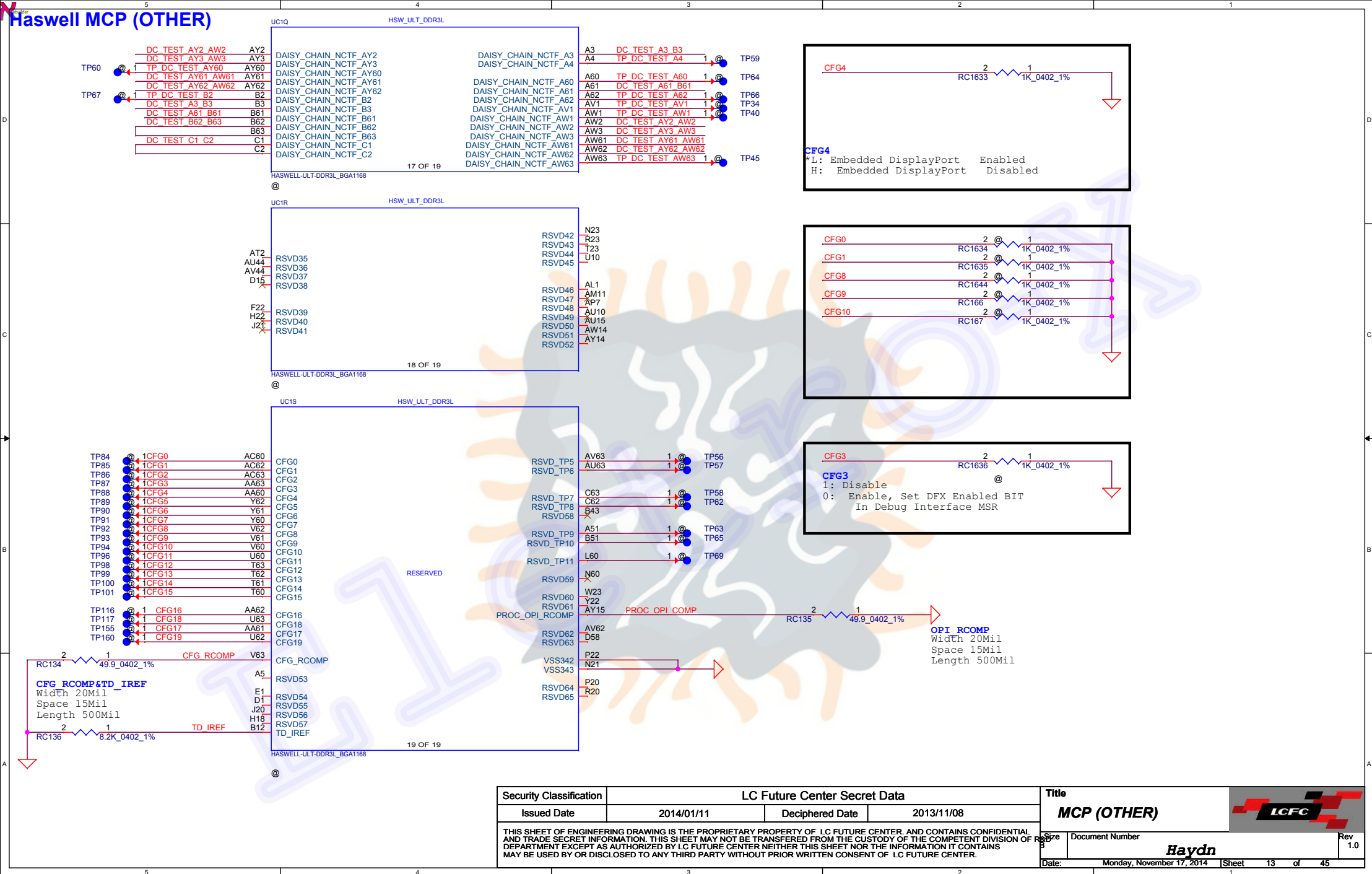


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MCP (Power)			
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# Haswell MCP (OTHER)





N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

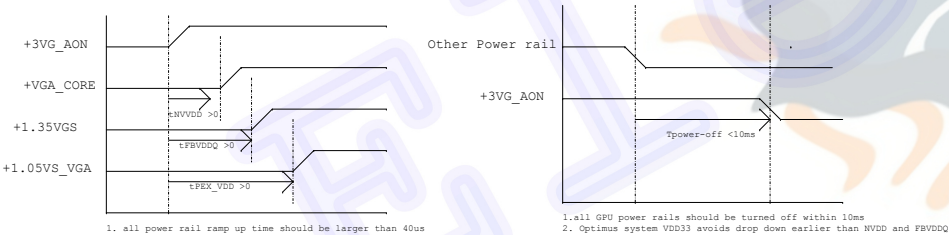
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.35V) (W)		FBVDDQ (GPU+Mem) (1.35V) (W)		PCI Express (1.05V) (s)		I/O and PLLVDD (1.05V) (mA)		Other (3.3V) (mA)	
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3 EXPOSED	SOR2 EXPOSED	SOR1 EXPOSED	SOR0 EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

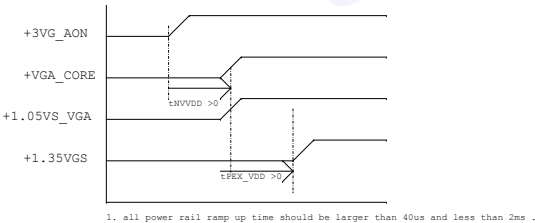
N15V-GM Power Sequence

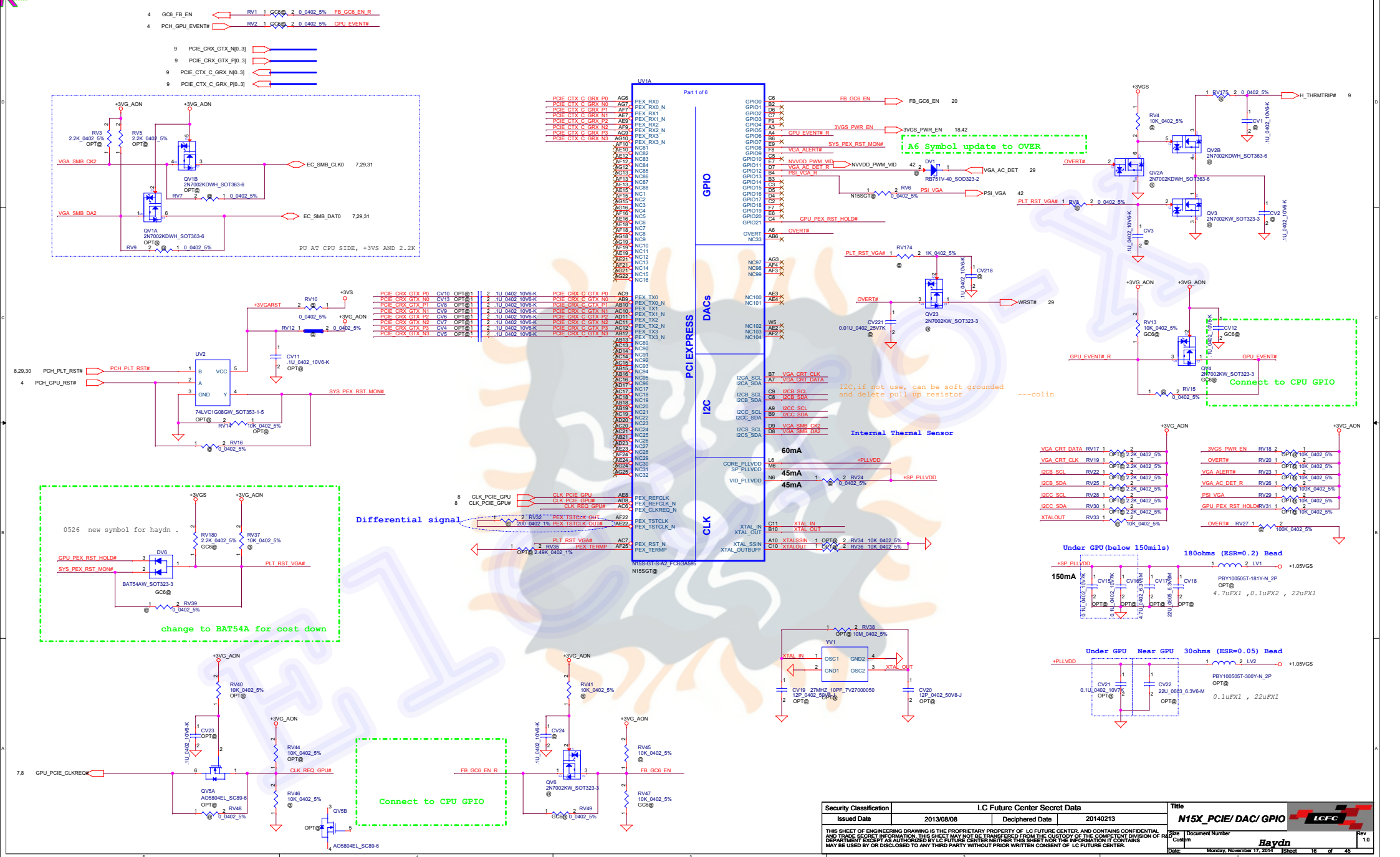


N15x Binary Straps

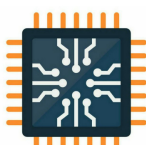
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

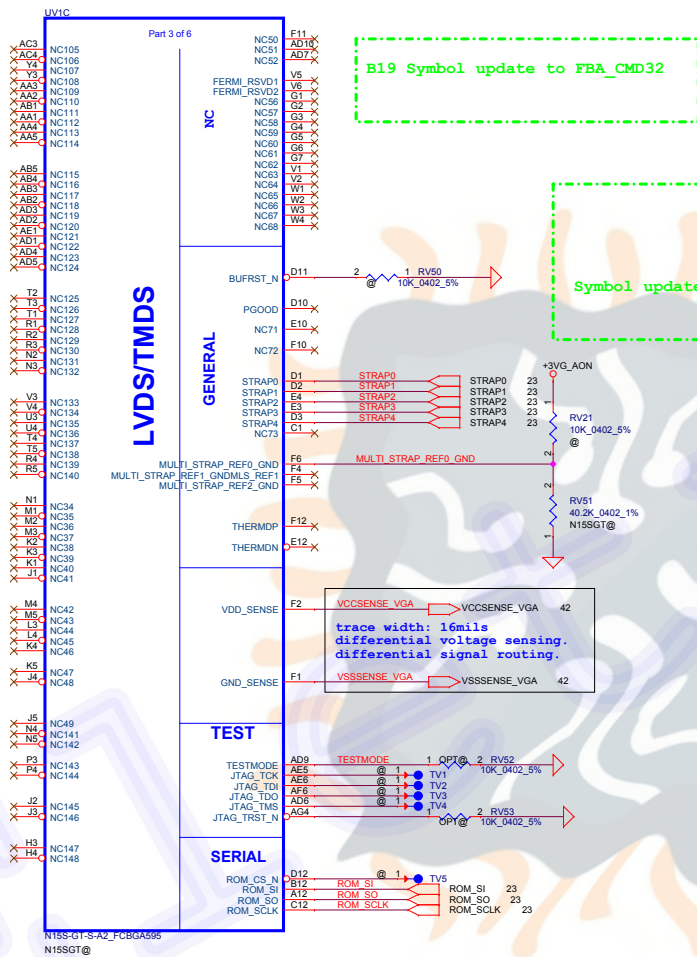
N15S-GT Power Sequence



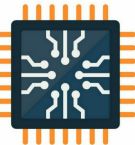
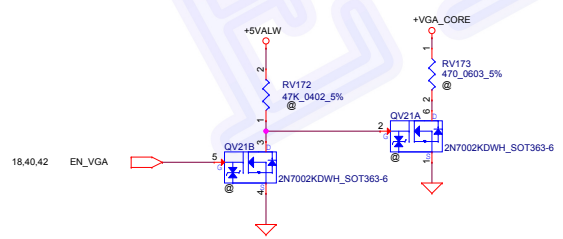
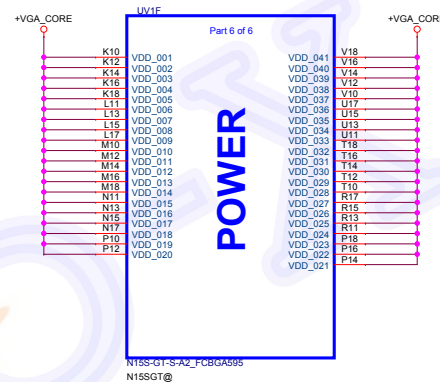
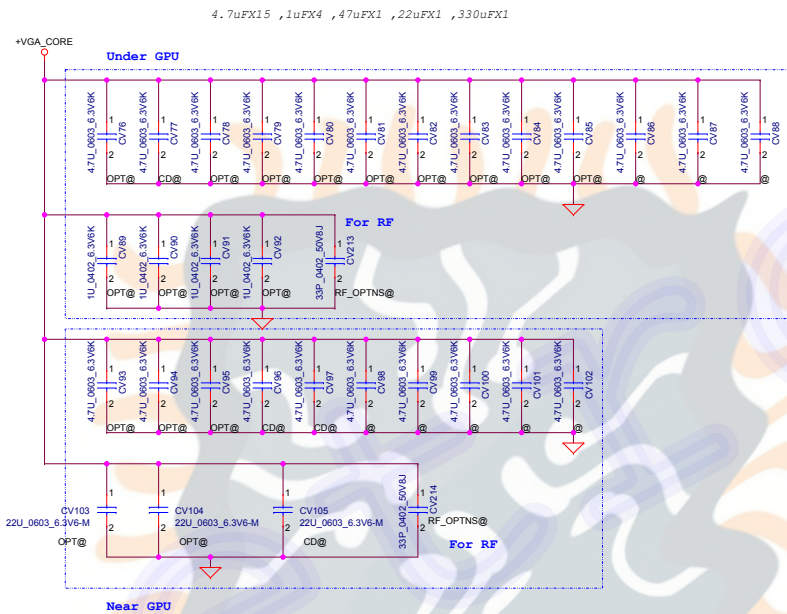
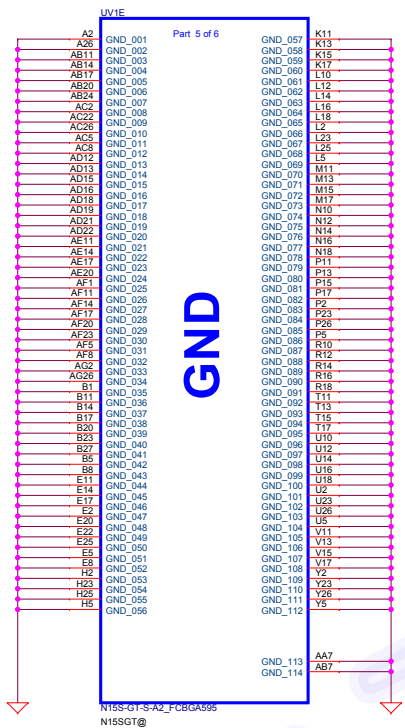


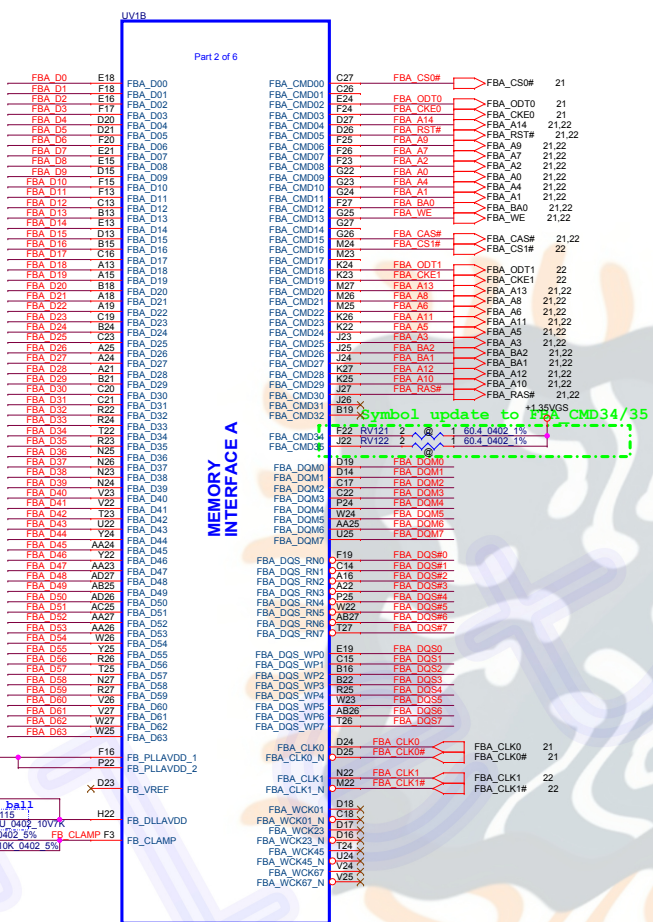
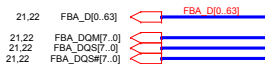
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		N15X_PCIE/DAC/GPIO	
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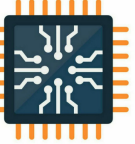
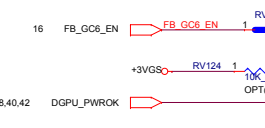
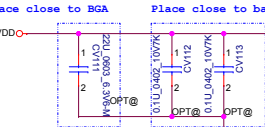
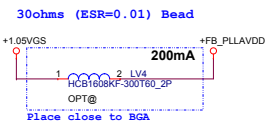




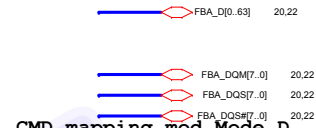
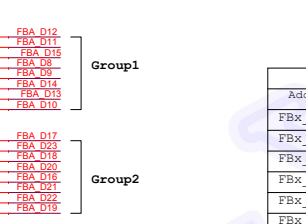
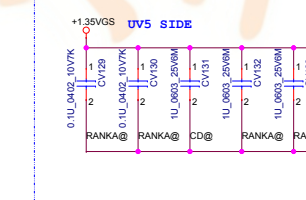
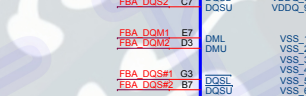
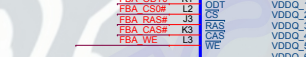
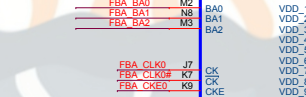
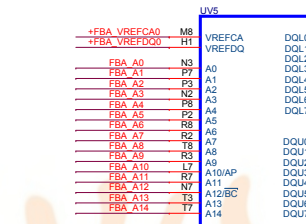
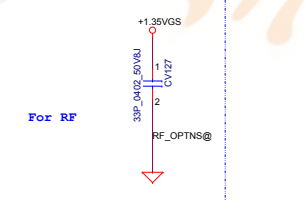
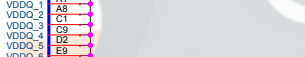
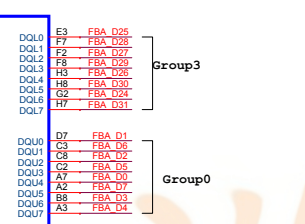
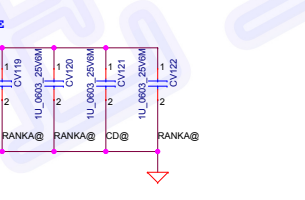
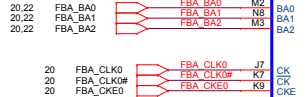
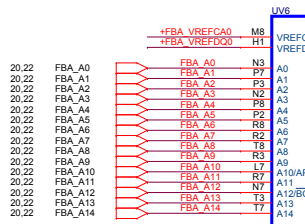
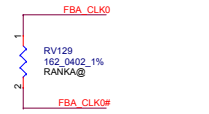
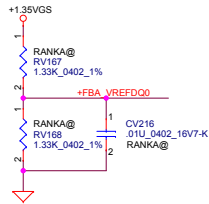
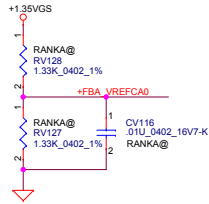


CMD mapping mod Mode D

Rank0			
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16	CSI#		
FBx_CMD17			
FBx_CMD18	ODT1		
FBx_CMD19	CKE1		
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		

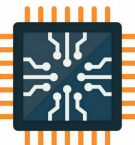


at least 16 mils width(optimal)  
20 mils spacing to other signals /planes

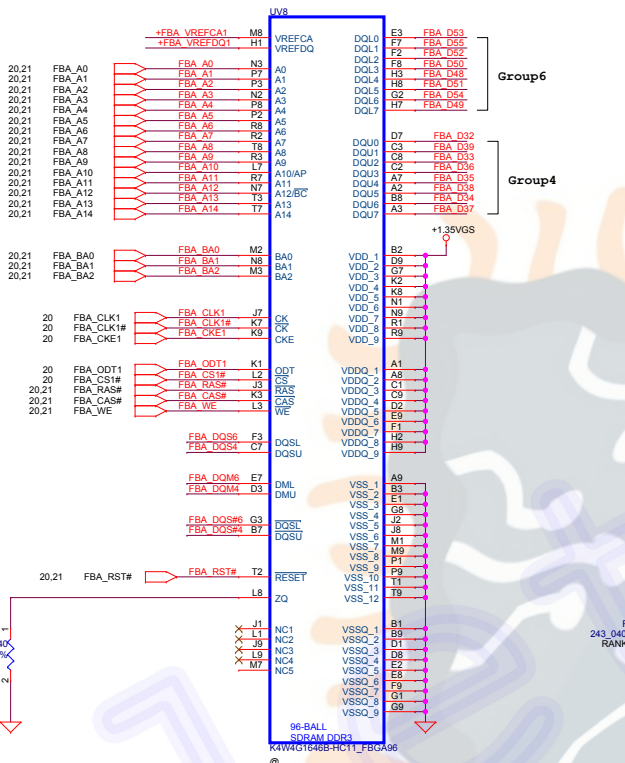
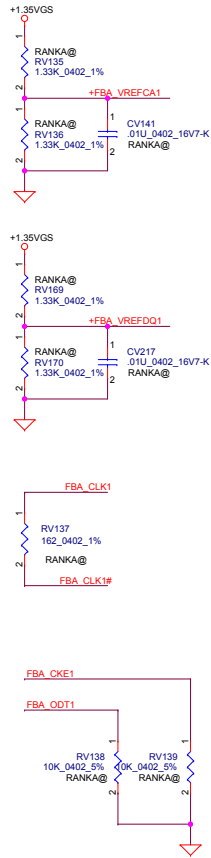


CMD mapping mod Mode D

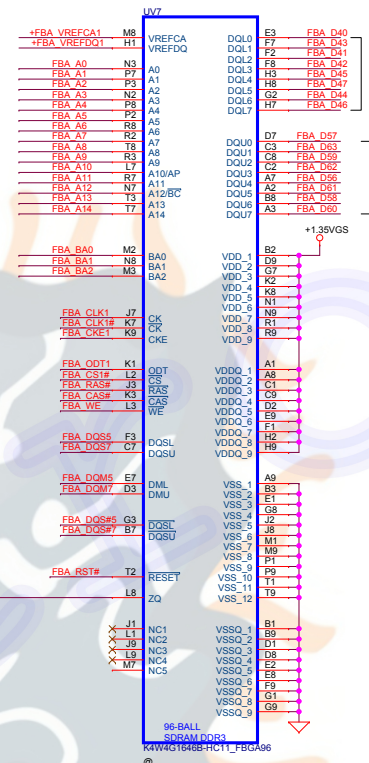
		Rank0	
Address	0..31	32..63	
FbX_CMD0	CS0#		
FbX_CMD1			
FbX_CMD2	ODT0		
FbX_CMD3	CKE0		
FbX_CMD4	A14	A14	
FbX_CMD5	RST	RST	
FbX_CMD6	A9	A9	
FbX_CMD7	A7	A7	
FbX_CMD8	A2	A2	
FbX_CMD9	A0	A0	
FbX_CMD10	A4	A4	
FbX_CMD11	A1	A1	
FbX_CMD12	BA0	BA0	
FbX_CMD13	WE	WE	
FbX_CMD14	A15	A15	
FbX_CMD15	CAS#	CAS#	
FbX_CMD16		CS1#	
FbX_CMD17			
FbX_CMD18		ODT1	
FbX_CMD19		CKE1	
FbX_CMD20	A13	A13	
FbX_CMD21	A8	A8	
FbX_CMD22	A6	A6	
FbX_CMD23	A11	A11	
FbX_CMD24	A5	A5	
FbX_CMD25	A3	A3	
FbX_CMD26	BA2	BA2	
FbX_CMD27	BA1	BA1	
FbX_CMD28	A12	A12	
FbX_CMD29	A10	A10	
FbX_CMD30	RAS#	RAS#	
FbX_CMD31			
FbX_CMD32			
FbX_CMD33			
FbX_CMD34	DBG0		
FbX_CMD35	DBG1		



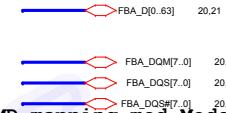
at least 16 mils width(optimal)  
20 mils spacing to other signals /planes



Group6  
Group4

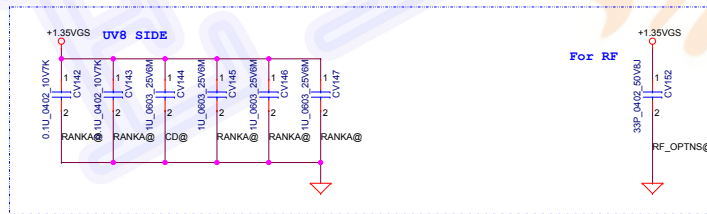


Group5  
Group7

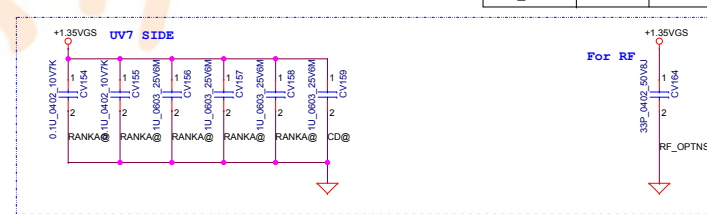


CMD mapping mod Mode D

Rank0			
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16	CS1#		
FBx_CMD17			
FBx_CMD18	ODT1		
FBx_CMD19	CKE1		
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		

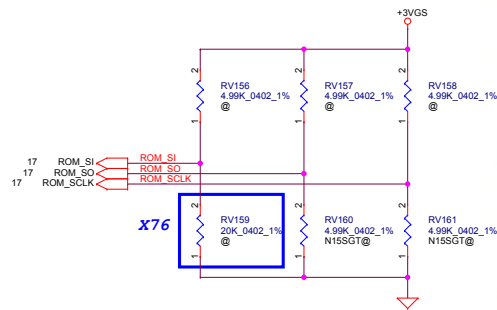
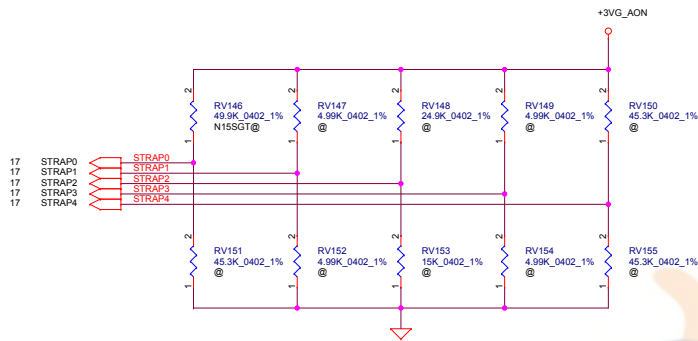


For RF



For RF





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

#### N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

#### X76

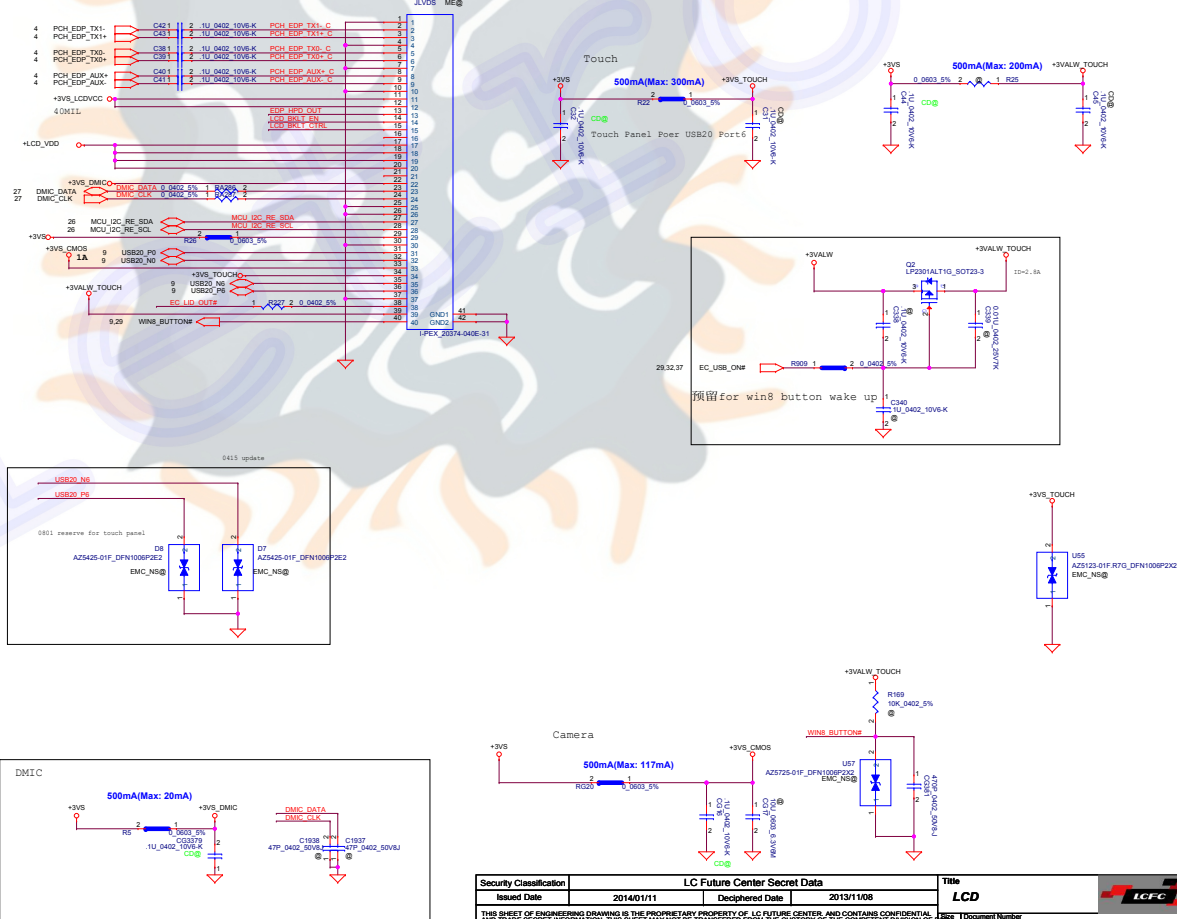
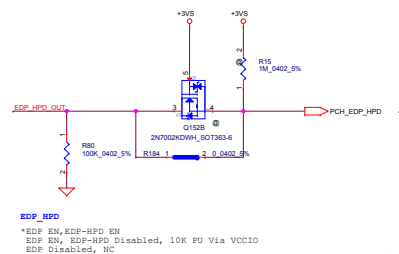
GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 20K							
	Micron 900MHz	MT41J256M16HA-093G:E	0x4							
		256M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A	0x5							
		256M x 16	PD 30.1K							
	Hynix 900MHz	H5TC2G63FFR-11C	0x9							
		128M x 16	PU 10K							
	Micron 900MHz	MT41J128M16JT-093G:K	0xA							
		128M x 16	PU 15K							
	Samsung 900MHz	K4W2G1646Q-BC1A	0xB							
		128M x 16	PU 20K							


VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

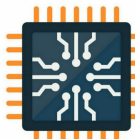


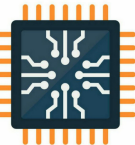
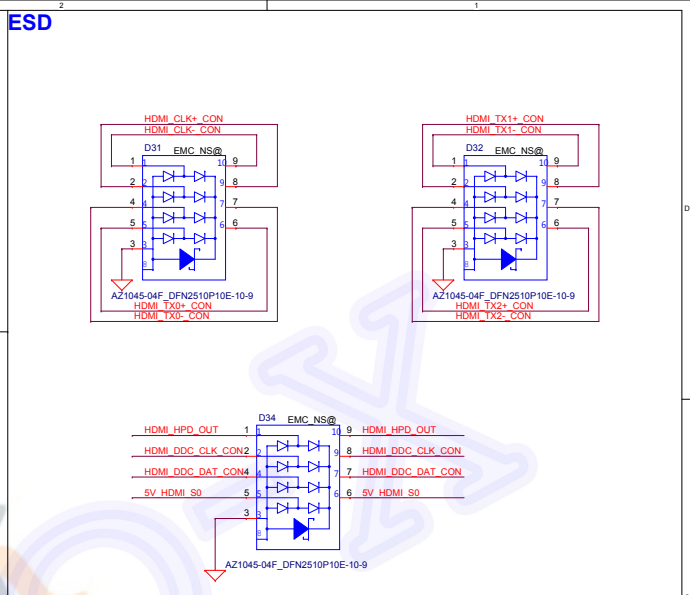
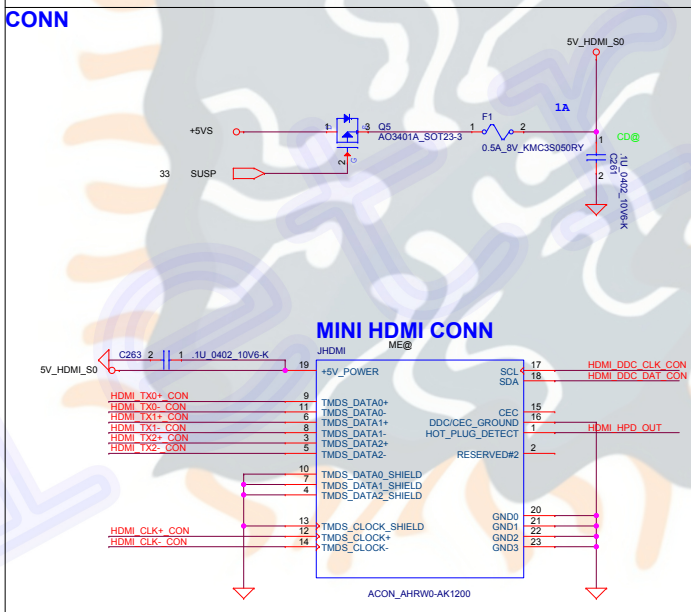
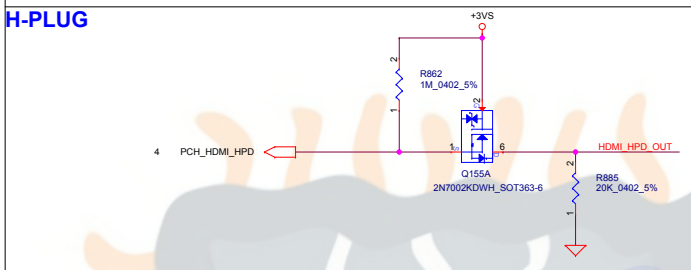
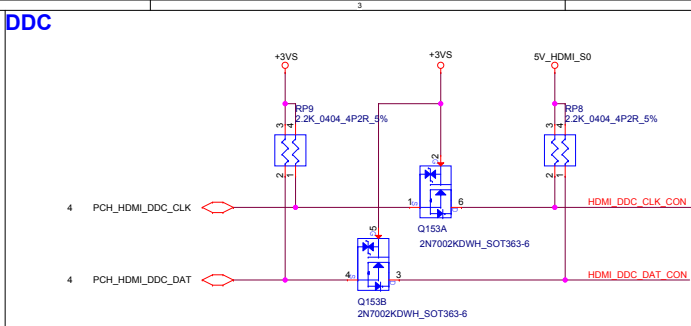
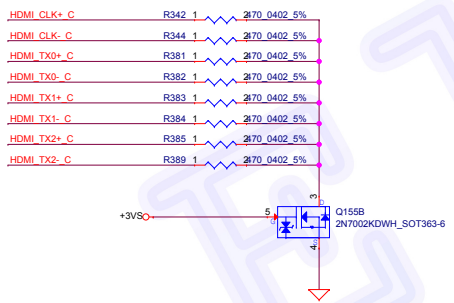
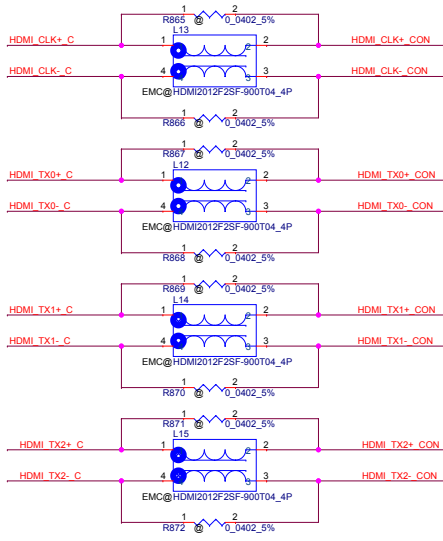
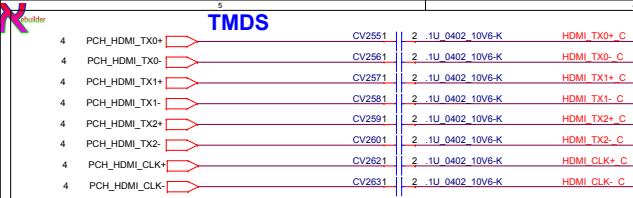


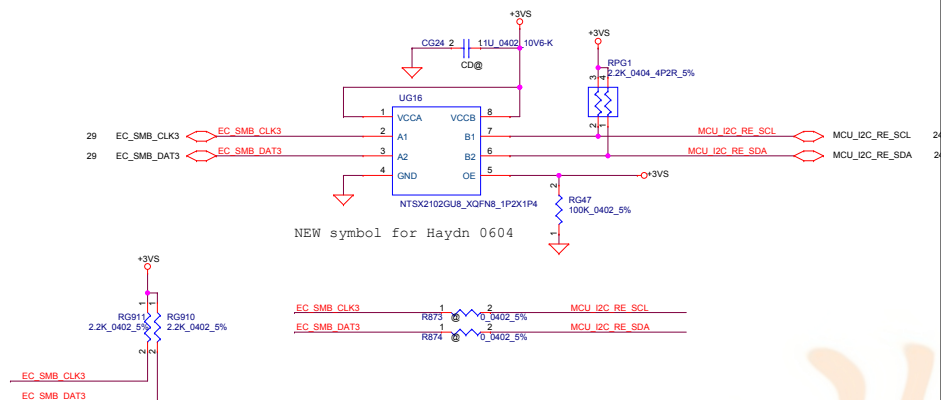
## BKLT CNTL



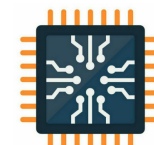
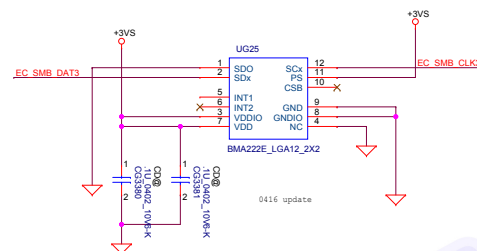
Security Classification	LC Future Center Secret Data		Title
Issued Date	2014/01/11	Deciphered Date	2013/11/08
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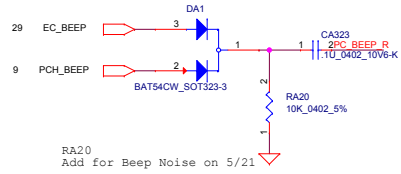




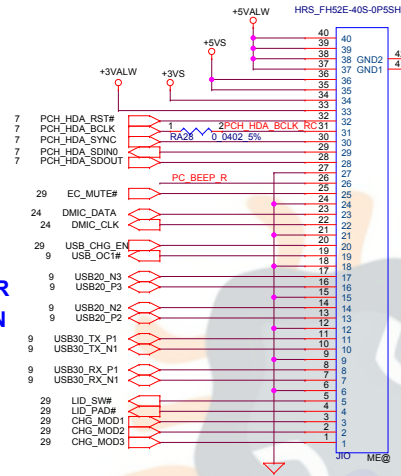
## G-SENSOR



# JIO HDA CARDREADER USB CONN

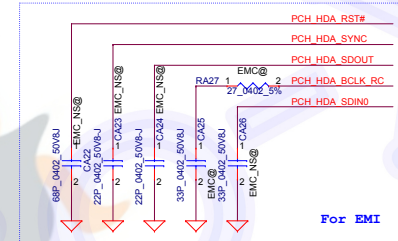
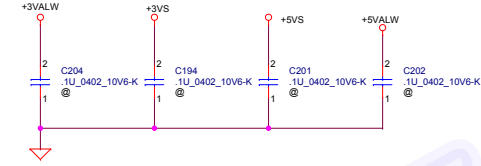


**CARD READER  
Left USB\_CONN**

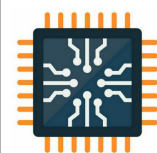
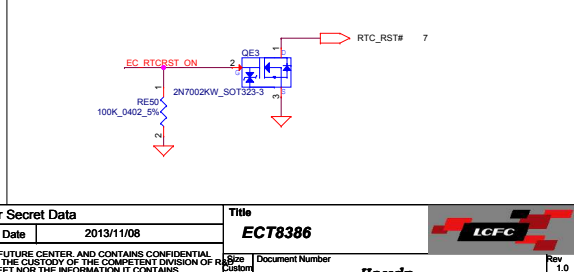
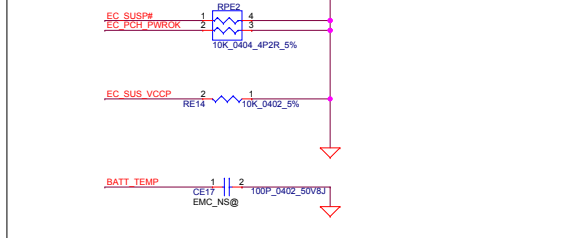
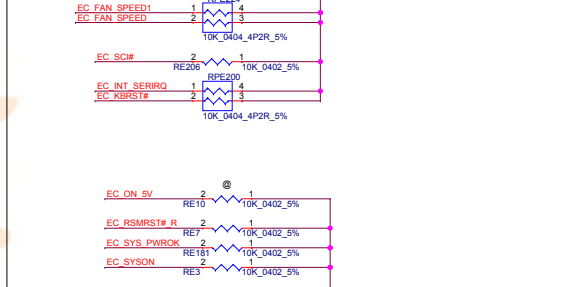
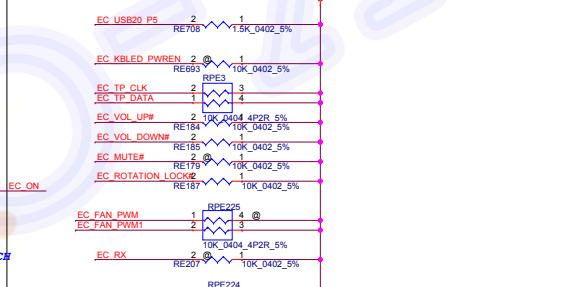
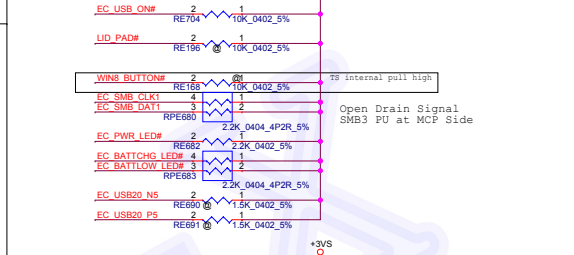
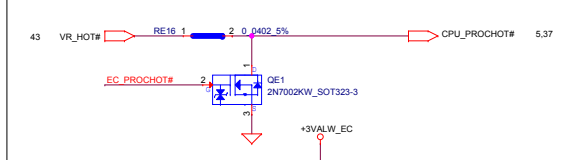
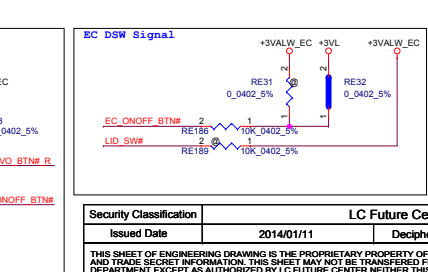
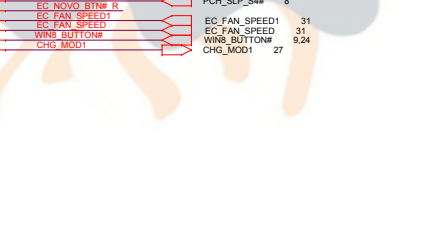
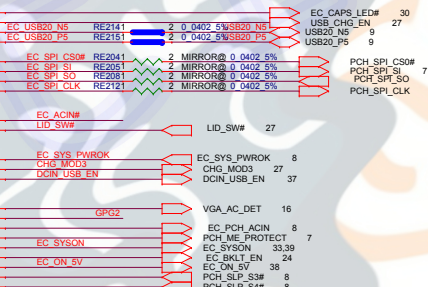
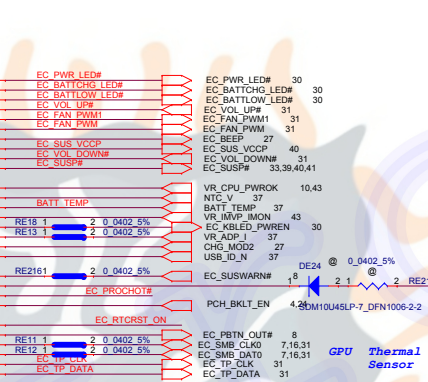
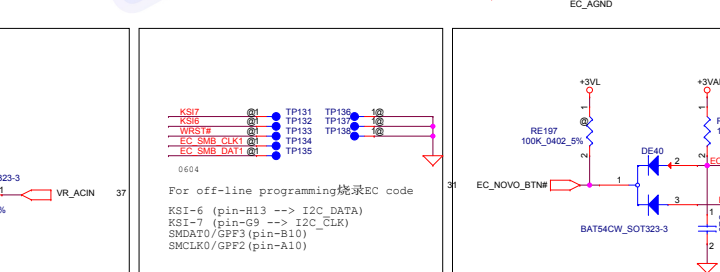
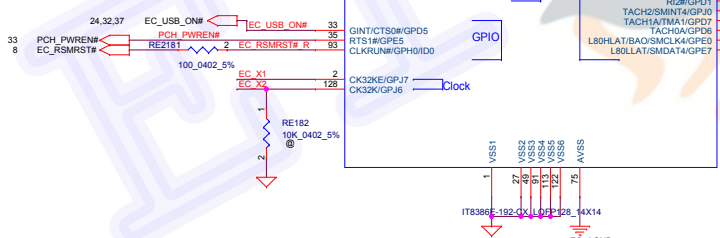
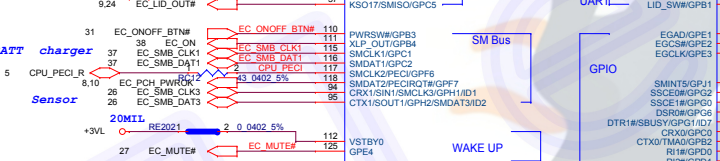
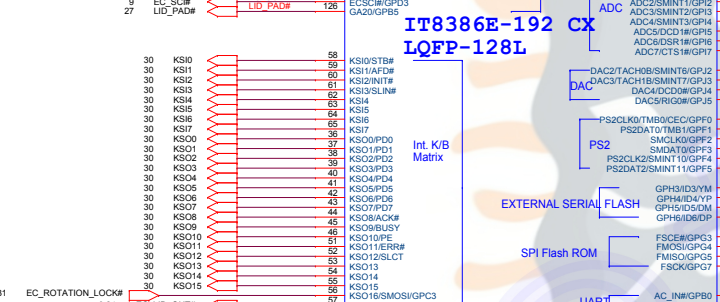
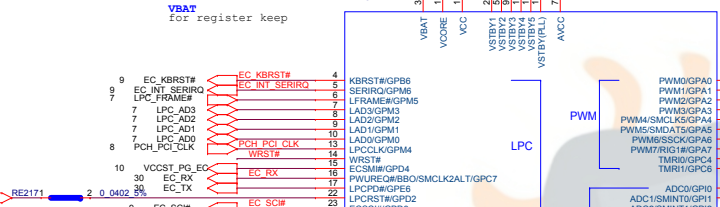
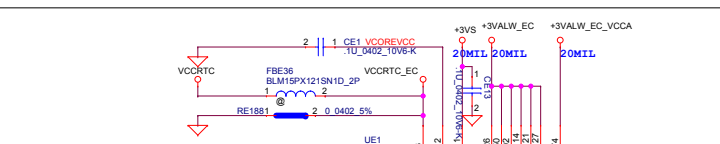
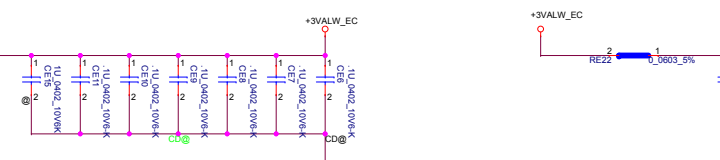
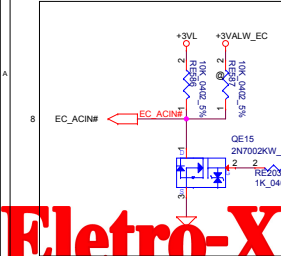
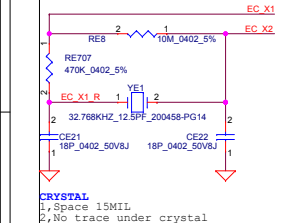
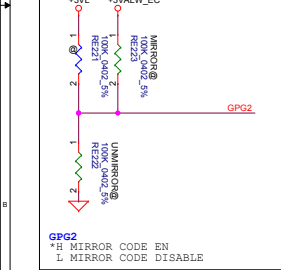
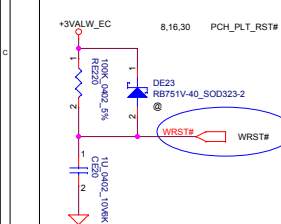
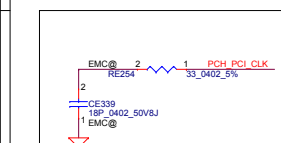
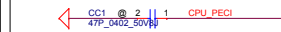


**RA28 Close to JIO**

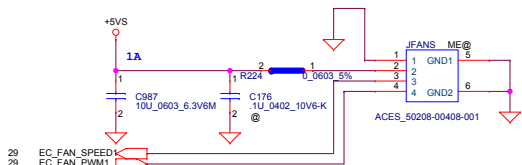
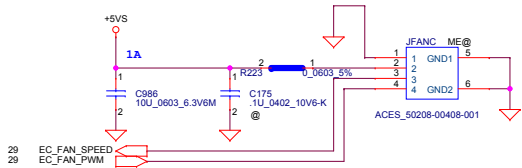
NEW symbol for Haydn 0609



8386

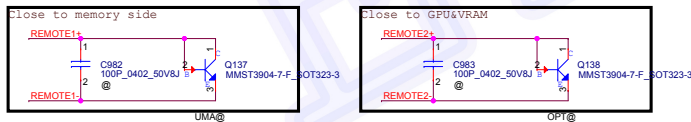
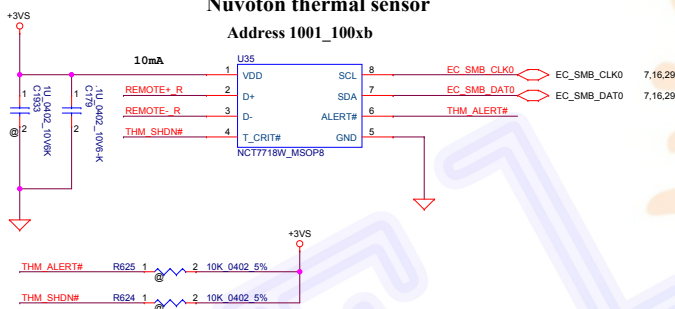




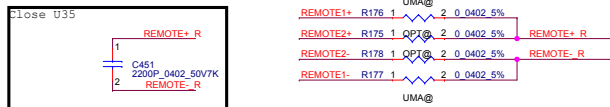


### Nuvoton thermal sensor

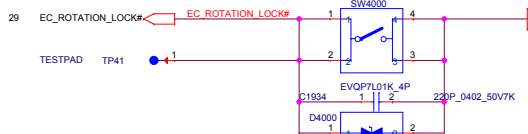
Address 1001\_100xb



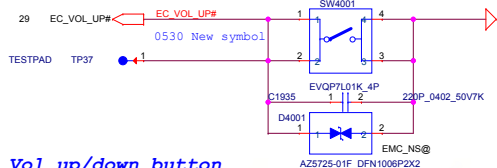
REMOTE1+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



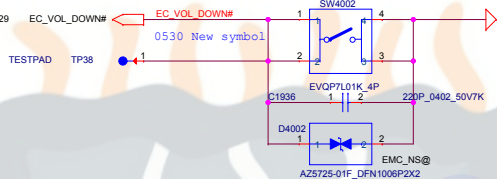
### Rotation button



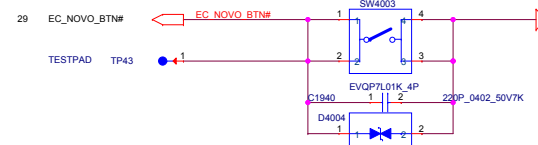
### Vol up/down button



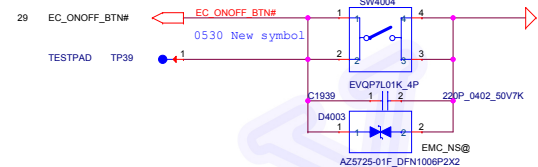
### Vol up/down button



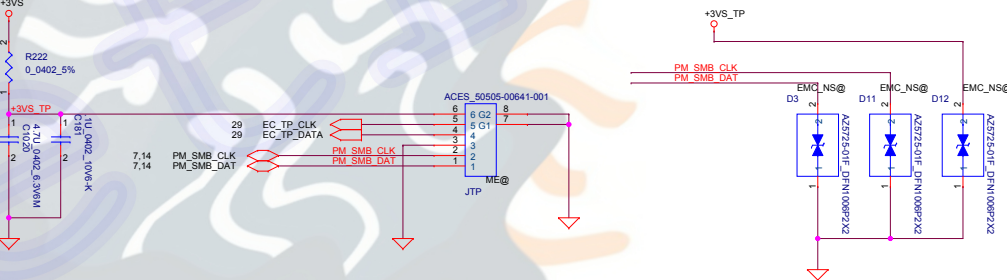
### NOVO button



### ON/OFF button

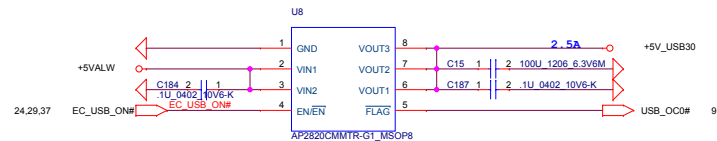
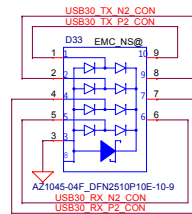
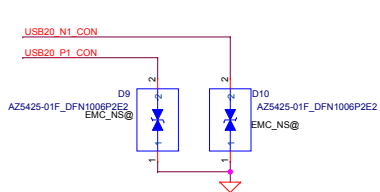
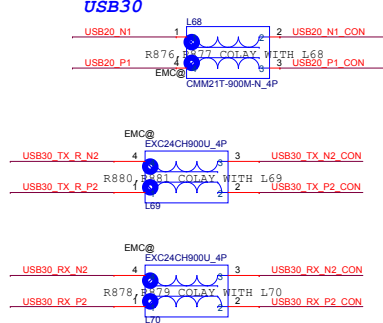


### Touch Pad Connector



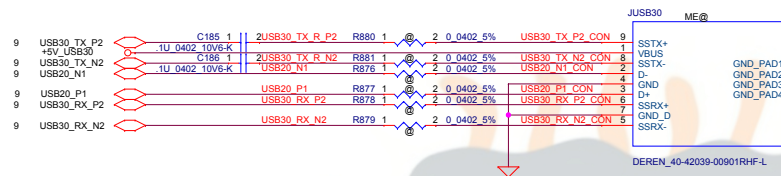
Security Classification	LC Future Center Secret Data		Title
Issued Date	2014/01/11	Deciphered Date	2013/11/08
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Date:	Monday, November 17, 2014	Sheet	31 of 45

### USB30

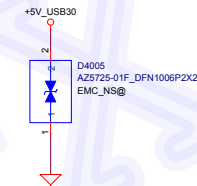


Low Active 2A

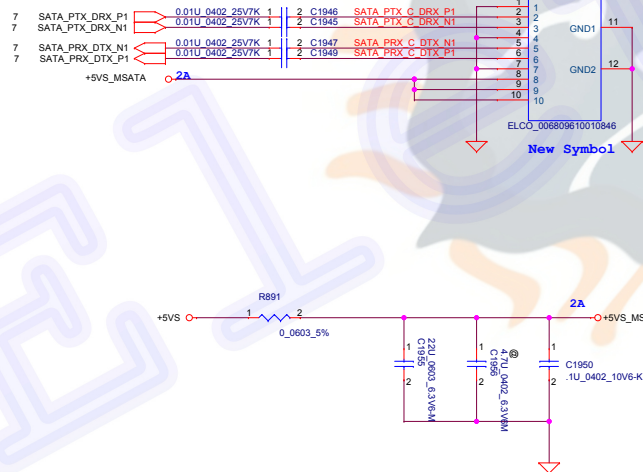
Left USB3.0/2.0



NEW symbol for Haydn 0604

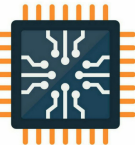
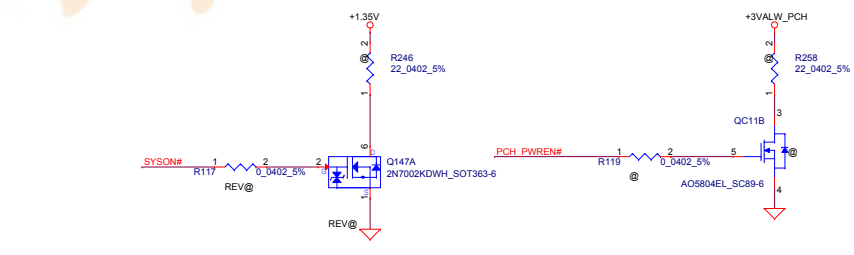
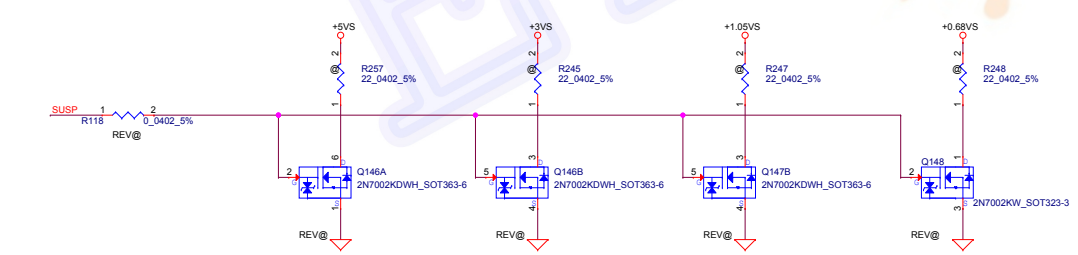
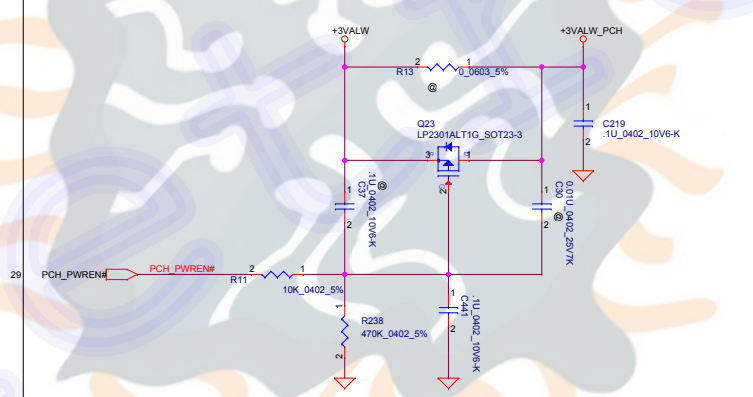
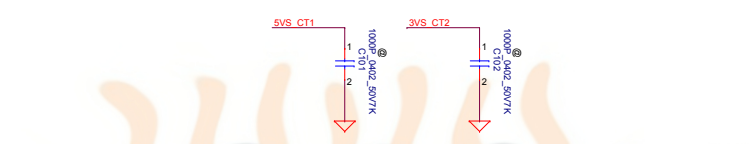
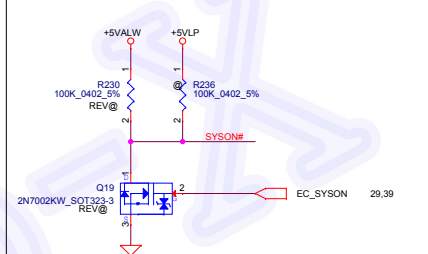
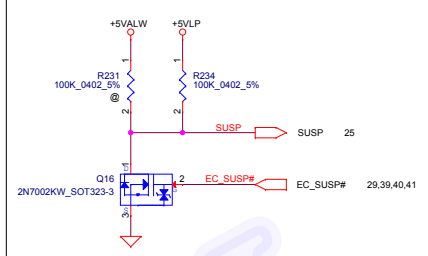
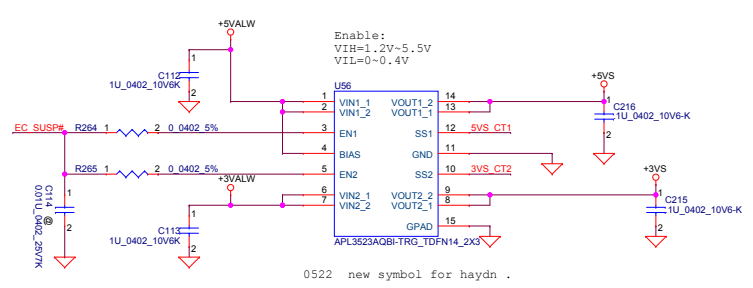
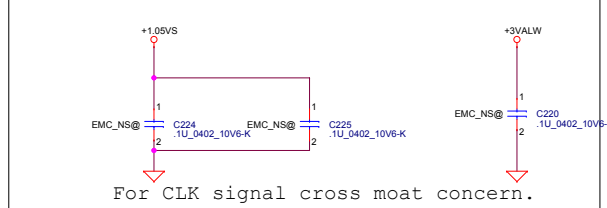
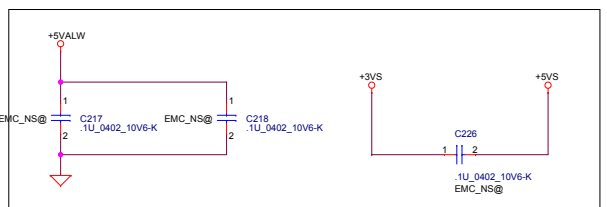
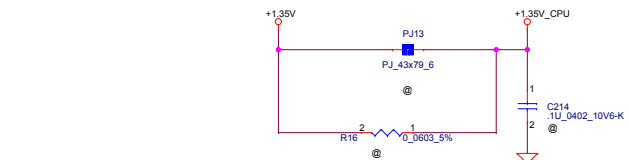


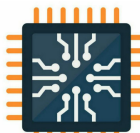
### MSATA (Full Card)



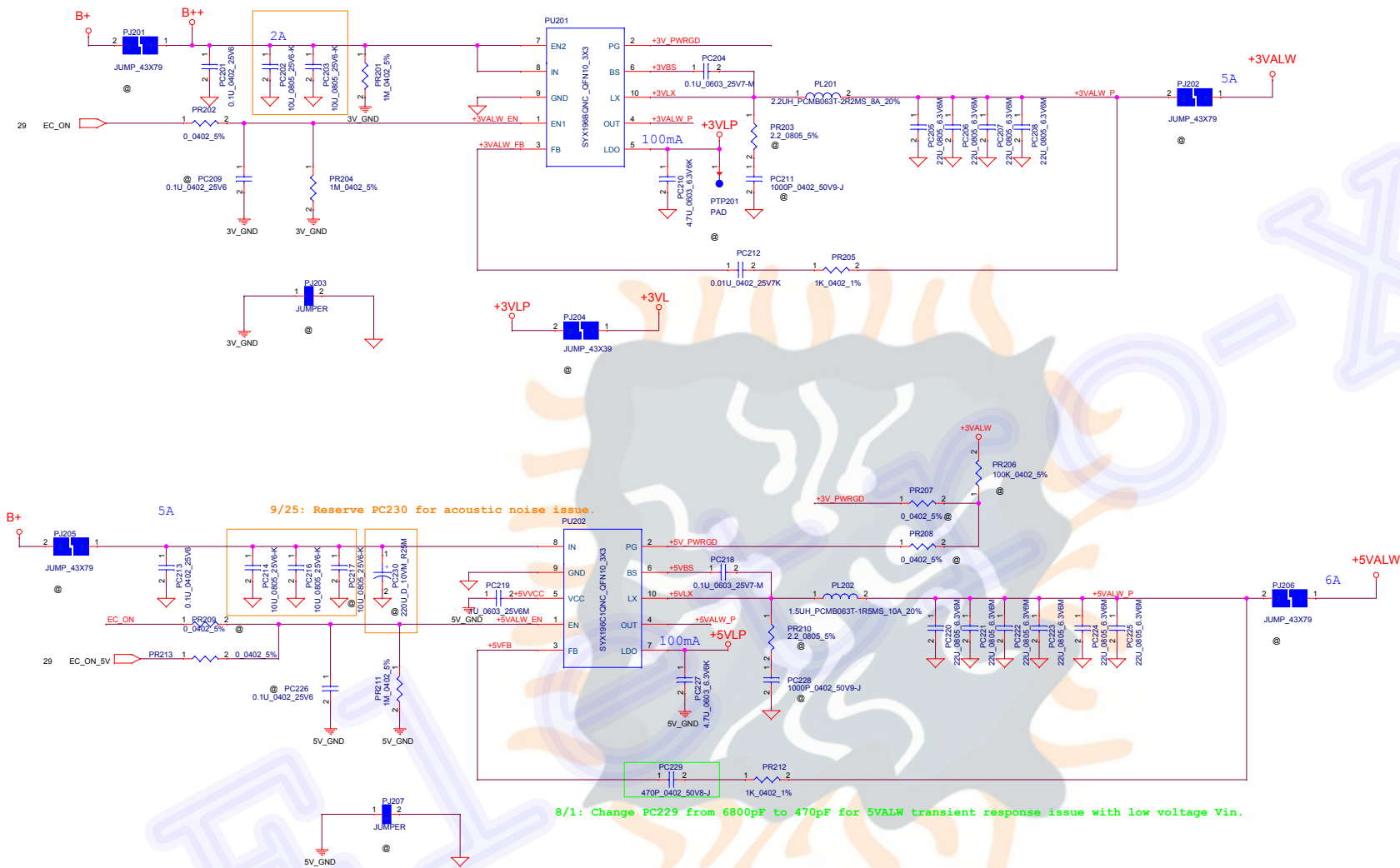
Security Classification	LC Future Center Secret Data		Title	CONN(MSATA&USB30&USB30) LCFC	
Issued Date	2014/01/11	Deciphered Date	2013/11/08	Document Number	Haydn
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9/25: Change PC202,PC203,PC214,PC216 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85.  
Reserve PC230 SGA00007I00 220U.  
To fix EE noise issue.

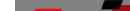


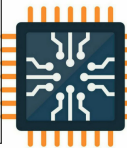
9/25: Reserve PC230 for acoustic noise issue.

8/1: Change PC229 from 6800pF to 470pF for 5VALW transient response issue with low voltage Vin.

3VALWP  
VFB=2V  
TDC 5A  
Fsw=350KHZ  
OCP: 7.8A~9.5A

5VALWP  
TDC 5A  
Fsw=300KHZ  
OCP: 7.8A~9.5A

Security Classification		LC Future Center Secret Data				Title	
Issued Date		2014/02/20		Deciphered Date		2014/02/20	
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						Document Number	
						Paganini	
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9/25: Change PC304,PC305 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85  
To fix EE noise issue.

4.9K\_0402\_1% SD00000H88J


9/25: Change PC304, PC305 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK0Q H0.85 To fix EE noise issue.

UMA SKU  
PQ302 change to AON7408L for 4A output current

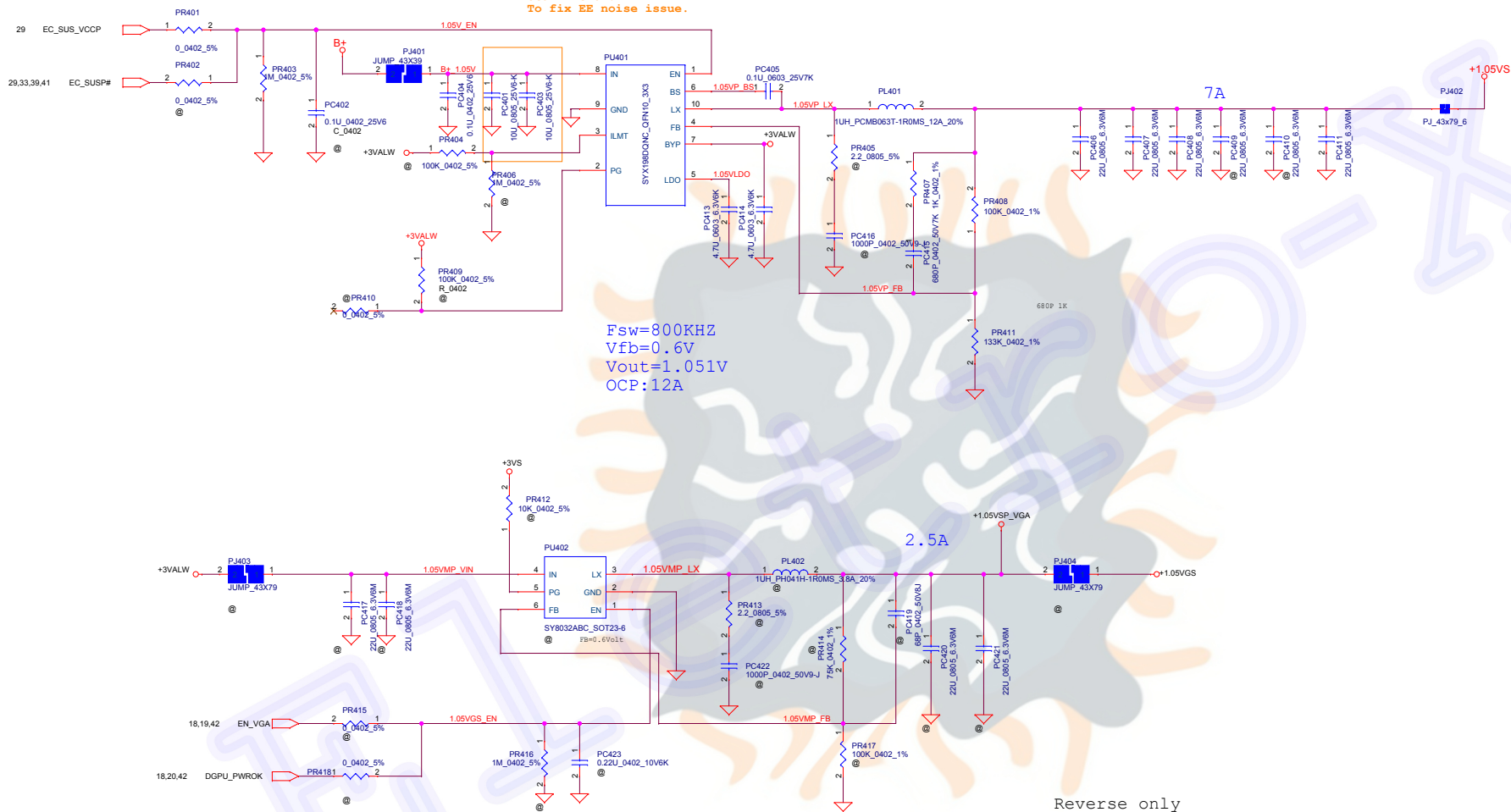
1.35VP  
Vout=1.367V  
Iocp min=13A fro DIS SKU  
Iocp min=6A fro UMA SKU

+1.35VP  
Vout=1.367V  
Iocp min=13A fro DIS SKU  
Iocp min=6A fro UMA SKU


UMA SKU  
PQ302 change to AON7408L for 4A output current

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2014/01/11		Deciphered Date		2013/11/08		PWR_1.35V/0.68VS			
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Date:		Monday, November 17, 2014		Sheet		39		of		45	

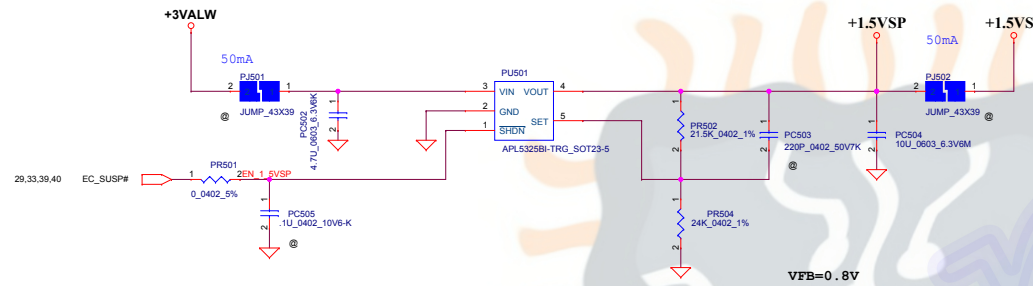
9/25: Change PC401,PC403 from SE00000QK0J 10U 25V 0805 H1.25 to SE00000QK00 H0.85.  
 Stuff PC401.  
 To fix EE noise issue.

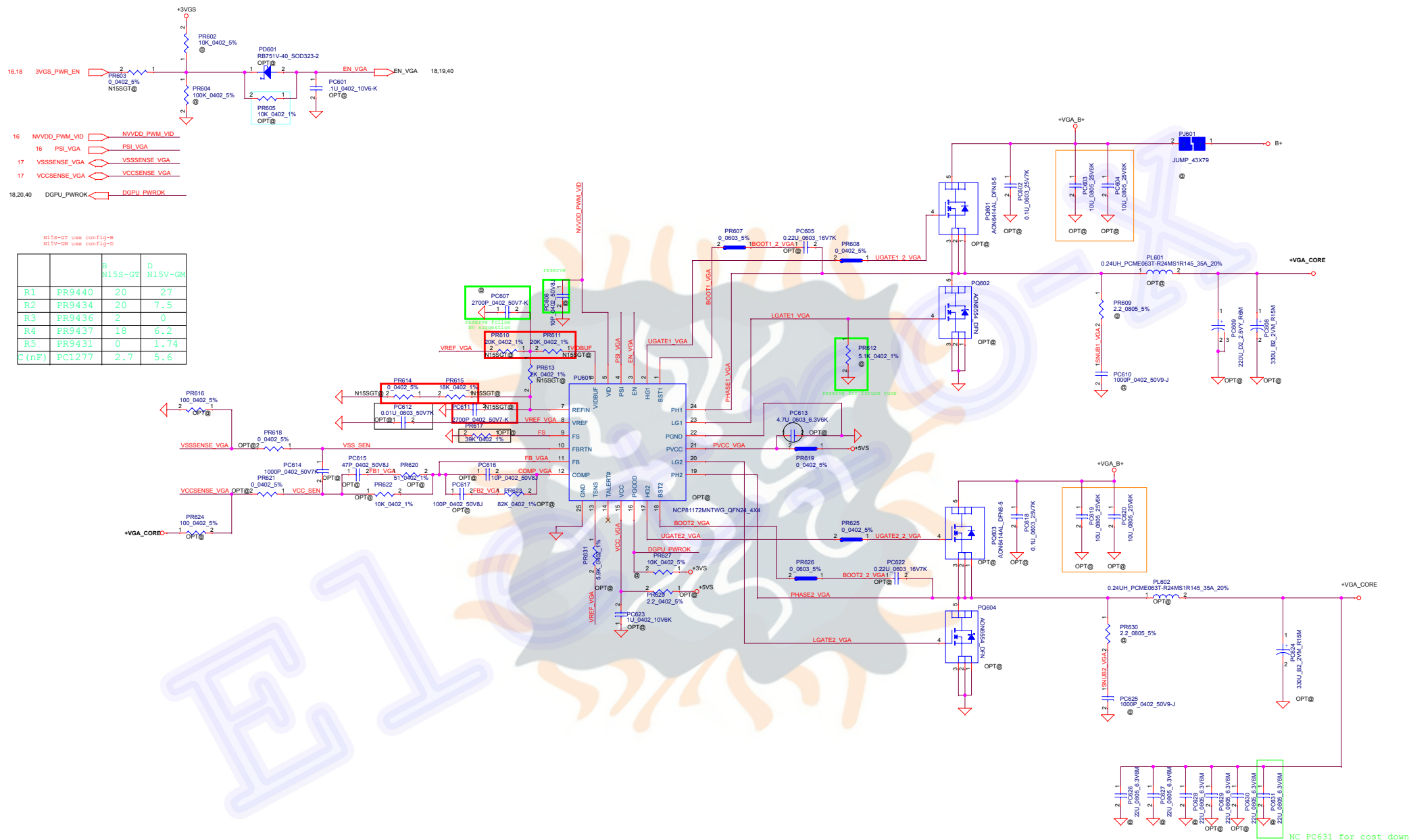



Reverse only

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2014/01/11	Deciphered Date	2013/11/08	PWR_1.35V/0.68VS		
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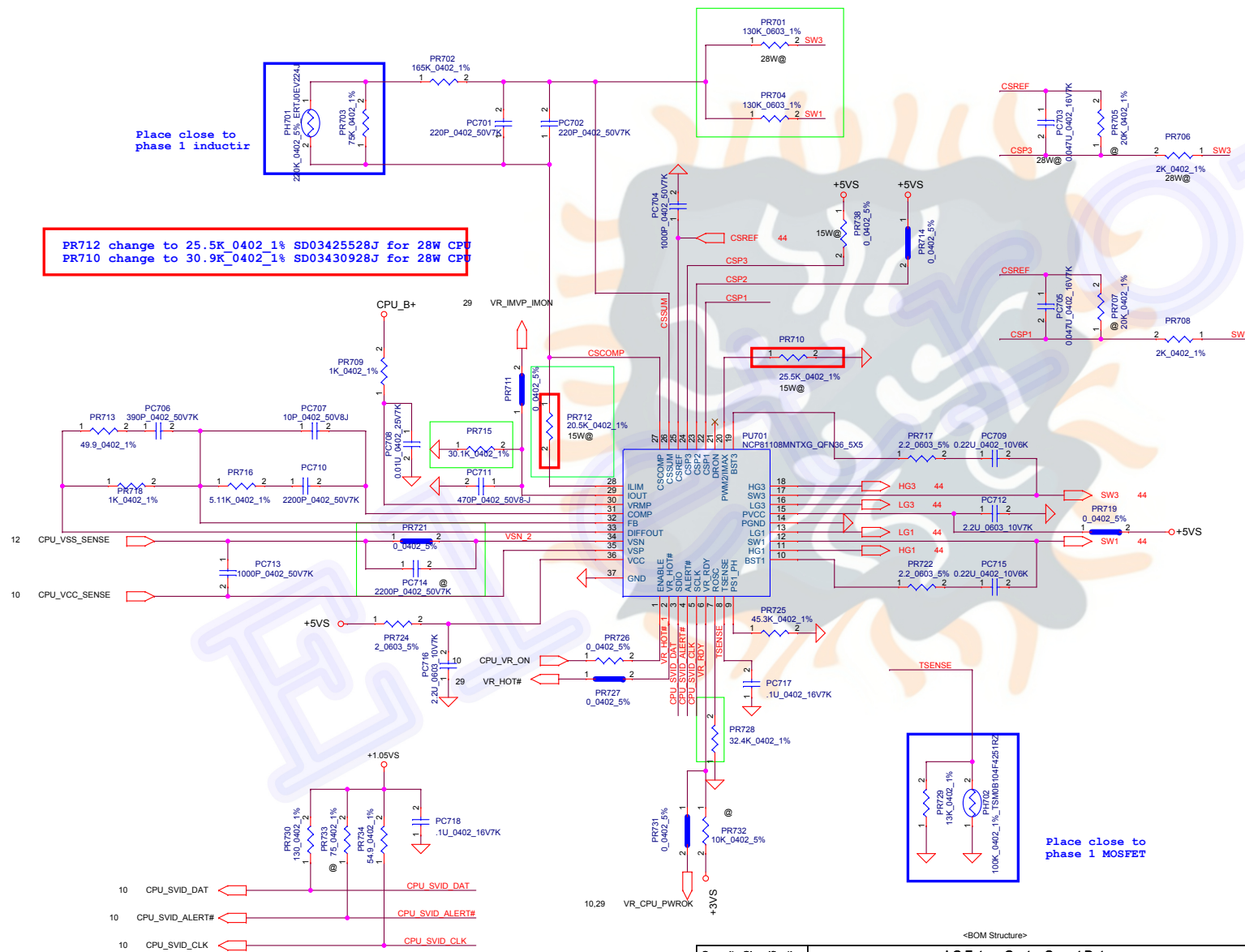






Security Classification	LC Future Center Secret Data		Title		
Issued Date	2014/01/11	Deciphered Date	2013/08/05		
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Document Number		Yoga3-BDW		Date	Monday, November 17, 2014
				Sheet	42 of 44

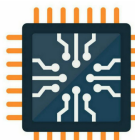


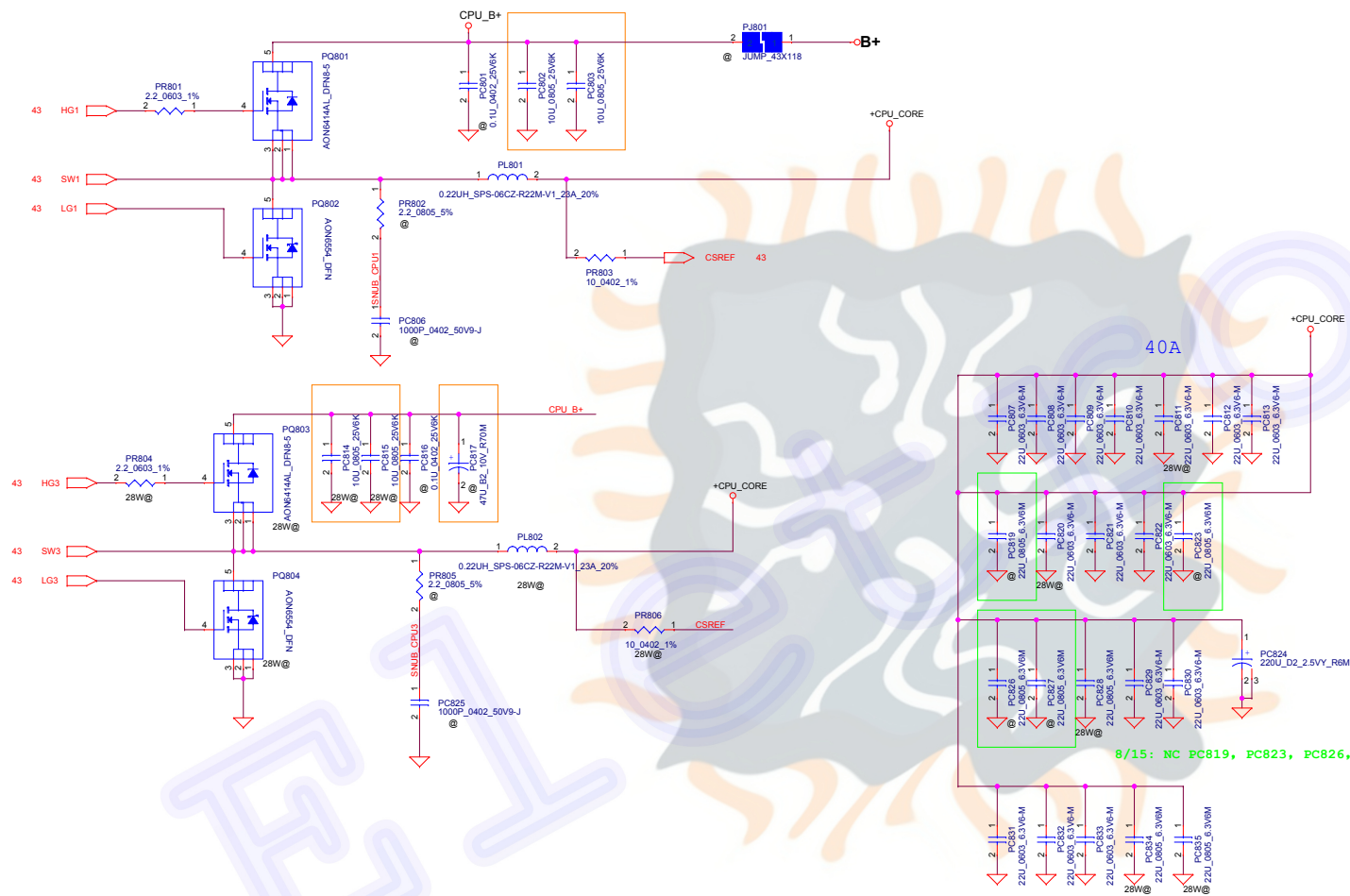


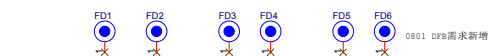
<BOM Structure>

Security Classification			
LC Future Center Secret Data			
Issued Date	2012/07/01	Deciphered Date	2014/07/01
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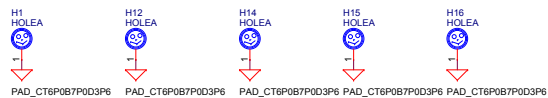
Title		Size	
CPU CORE		Document Number	Rev 1.0
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PAD\_CT6P0B7P0D3P6



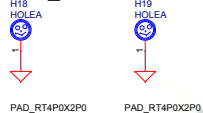
PAD\_CT6P0



PAD\_C7P0D4P3



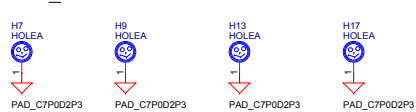
PAD\_RT4P0X2P0



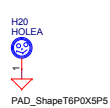
PAD\_C7P0D5P6



PAD\_C7P0D2P3



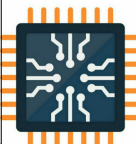
PAD\_ShapeT6P0X5P5



PAD\_O2P7X2P2D2P7X2P2N



PAD\_C2P2D2P2N



4/16:  
1.EDP connector change to 40 pin , touch connector change to 10pin .  
2.5 sensor change to BMA222E  
3.Modify DIMM connector pin define

4/24:  
1.CV112 change to 0.1uF follow DG.

4/28:  
1.unstuff pull up pull down resistor for GPU CMD signal (Single rank no need)  
2. Reserve pull down resistor for signal OVER#  
3.reserve pull up resistor for signal MULTI\_STRAP\_REF0\_GND

4/29:  
1.use buffer for signal CPU\_DRAMPG\_CNTL

5/4:  
1.Delete N15VGM# part for Haydn only support N16S-GT.

5/6:  
1.VR ADP ID change to USB ID N  
2.EC ADP ID ON# change to DCIN USB\_EN  
3.Delete GPU CMD signal pull up/pull down resistor  
4.update EC to LQFP package  
.

5/8:  
1. Change YC1,YE1 to 32.768KHZ 12.5PF\_200458-PG14  
2. Stuff QV7 for GPU +1.05V power  
3.Add one BJT on thermal sensor for GPU&VRAM  
4. Change YC1 to 32.768KHZ 12.5PF\_202740-PG14

5/9:  
1. modify HDMI DATA signal connection .  
2. renaming GPU command signal  
3.mount RC762, unmount DC27 for cost down .

5/11:  
1.Change UE1 to IT8386E-192-CX LQFP128 for cost down  
2.Change YC2 to 24MHZ 6PF 7V24U00032 for cost down  
3.Change D4,D5,D6,D13 to ESD9N5BL-2-TR\_DFN1006-2 for cost down

5/12:  
1.Change JWLAN to LCN\_DAN05-67146-0102  
2.Delete JRTC  
3.Change CC130 to SE00000P10J for cost down  
4.Change D31,D32,D33 to AZ1045-04F for cost down

5/14:  
1.Change R105 to 1K ohm.  
2.Change CC44 to SGA00009900 for layout placement concern .  
3.Change QV8,QV17,QV21 to 2N7002KDWH for layout placement concern .

5/15:  
1.Change JFANC ,JFANS to 88231-04001 follow ME connector list .

5/19:  
1.Touch Pad change to I2C interface.  
2.Haydn support two FAN ,connect the two FAN signal to EC .  
3.Delete one debug connector JDB3.  
4.delete deep S3 schematic part .  
5.Modify KB pin define .

5/20:  
1.Move lid\_pad# part schematic to USB DB .

5/21:  
1.Change D34 to AZ1045-04F DFN2510P10E-10-9 follow EMC suggestion .  
2.Change D7,D8,D9,D10 to AZ5425-01F follow EMC suggestion .  
3.Delete SPI rom power control part schematic since not support DS3 now .  
4.Touch screen part function use the same connector with EDP .

5/22:  
1.Use cost down solution for signal CPU\_DRAMPG\_CNTL follow G .  
2.Change U56 to APL3523AQBI-TRG for cost down.  
3.Change JKB to ACES\_50506-0260M-001 follow ME connector list .

5/26:  
1.Change DV5,DV6 to BAT54AM\_SOT323-3 for cost down.  
2. Reserve JRTC  
3. modify JLVDS pin define .  
4.Delete reserved components QV24,QV25 ,DV5 for signal VGA\_PWRGD

5/27:  
1.Reserve CC110 for signal +1.05VS DCP5US4  
2.Change JKB to ACES\_50519-02601-001 follow ME connector list .  
3. Change JTF to ACES\_50503-0060M-001 follow ME connector list .  
4. Delete WLAN AQAC part schematic .  
5. Swap VRAM data group 2 ,group3 and Swap VRAM data group 6 ,group7 for layout routing concern .

5/28:  
1.Reserve USB3.0 signal that connected to JIO.  
2.Reserve R873,R874 for the possibility to cost down I2C redriver.  
3.Change QV10,QV13 to 2N7002KDWH for layout placement concern .  
4. Swap VRAM data group 4 ,group5 for layout routing concern .  
5.Change R8710 to R8710 and R8711 for layout concern.

5/29:  
1.Reserve RV39 ,RV171 follow NVIDIA suggestion.  
2.Modify JIO pin define ,add USB charger mode control signal .

0603:  
1.Change JFANC ,JFANS to ACES\_50208-00408-001 follow ME connector list .  
2.Delete ECIE WAKE#,PCH ACIN.--reserved pull up signal +3VL for layout concern.  
3.Delete QV13",Change QV12,QV19 to 2N7002KDWH\_SOT363-6 for layout concern.

0604:  
1.Change JUSB30 to C-K 26211-8B19-02 follow ME connector list .  
2.Change UG16 to NTSX2T02GUS\_XQFN8 for cost down.  
3.Delete reserved component CC44 for layout concern.  
4.update hole symbol.

0606:  
1.Change HDMI part 0.1uF cap to 0402 size Follow DG.  
2.Add reserved Caps for keyboard signal follow EMC suggestion.  
3.Add reserved Caps for HDA signal follow EMC suggestion

0607:  
1.Combine EC part resistor for bom quantity concern.

6/9:  
1.Change JHDMI to AHRW0-AK1200 follow ME connector list .  
2. Change JTF to 50505-00641-001 follow ME connector list  
3.Change JIO to ACES\_51540-04041-001 follow ME connector list .  
4. Change JWLAN to LOTES\_APCI0062-P007A follow ME connector list .

6/10:  
1.Modify JLVDS pin define.  
2. Add signal ILIM\_SEL for USB charger.

6/12:  
1.Change LV2 to PBY100505T-300Y-N ,LV1 to PBY100505T-181Y-N For smaller size.  
2.Reserve RTC\_RST# schematic controlled by EC.  
3.Modify EC pin define(Four signals.)

6/16:  
1.Change button switch SW4000,SW4001,SW4002,SW4003,SW4004 to EVQP7L01K\_4P.

6/17:  
1.Change QV5, QC13, QC12, QV10 to A05804EL SC89-6 for layout concern.  
2.Change CV22,CC121,CC130,CC131, CV103, CVI04, CV105 to SE00000M00J for layout concern.

6/18:  
1.Modify GPU power on sequence .  
2.Change CV111 to SE00000M00J ,CV60 to SE107475K0J for layout concern.  
3.Add thermal protection schematic .  
4.Change QC11,Q149 to SB00000XP0J for layout concern.

6/19:  
1.Delete thermal protection schematic dummy components since no space to placement .

6/20:  
1.Add C217,C218,C220,C224,C225,C226 For CLK signal cross moat concern .  
2.Delete JCMOS1 ,add test point for signal RTC\_RST#

SIV

7/21:  
1.Delete CG380 For CG380/CG381 function repetition  
2.Delete RV70,RV61 +1.35VGS/+1.05VGS Mosfet control signals power level change  
3.Change CV54 from 0.1uf to 0.01uf. RV228 from 560ohm to 0ohm. CV506 from 0.1uf to 0.22uf for GPU power sequence change  
4.Change touch pad to SMBUS solution.

7/29:  
1.Delete QC5 (not connect to PCH)  
2.Change RE218 from 0ohm to 100ohm for EC RSMRST# overshoot/undershot fail  
3.Add CC50 0.01uf for VCCST PG EC\_R undershot fail  
4.Change RC61 from 0ohm to 100ohm for SYS\_PWROK overshoot/undershot fail  
5.Change CC23,CC24 to 2.7pF ,CV19,CV20 to 12pF follow crystal vendor suggestion.  
6.Change RE707 to 470K ,CC7 to 15pF follow crystal vendor suggestion.

08/05:  
1.modify EC GPIO (EC\_ON)

08/07:  
1.JLVDS rotate 180 degree

08/11:  
1.Change 0 ohm resistor (RC65,R184,RE188,R351,RC761,RD16,RD22, RE32, RC97, R110, R125,R121,R126  
RC138,RE202,RE217,RC31,R109,R113,R114,RC758,RC759,RC105, RC103,RC99) to jump  
2. NO stuff CE6 ,CD88

08/11:  
1.Mount RA27 ,CA25 Follow EMC suggestion.  
2. Change JIO to HRS FH52E-408-0P5SH follow ME suggestion.  
3.Change JSATA to ELCO\_006809610010846 follow ME suggestion.

SIT

9/23:  
1.Change JLVDS to I-PEX 20374-040E-31 follow ME suggestion.  
2.Change some power plane from +3VALW to +3VALW\_PCH.  
3.Mount D13 follow emc suggestion.

9/24:  
1.Reserve CC31 and CC32 For EMC.

9/25:  
1.Mount RE254 ,CE339 For EMC.  
2.Change RE22 , RE23 ,RC62 ,RC81 ,RC85 ,R909 ,R223,R224 to R short.  
3.Change L69,L70 to EXC24CH900U for cost down

10/13:  
1.Change CC23,CC24 to 3.3pF for RTC Time test fail in windows.

11/11:  
1.Change CE339 to 18pF for HSW platform LPC CLK fall slew rate test fail issue.

11/13:  
1.Change R2,R22,R5,R13,RC20,R26,RC107,RC122,RC124,RE214,RE215,RE216 to R short for cost down.  
2. Mount RE50,QE3,Q23,R11,R238,C441 for clear CMOS.  
3.Change JWLAN to DEREN 40-42313-06742RHFL follow ME request.  
4.Change JUSB30 to DEREN\_40-42039-00901RHF-L Follow ME request.

